iC-PI PROGRAMMABLE 12-BIT
Sin/Cos INTERPOLATION IC WITH RS422 DRIVER

FEATURES

- Latency-free sine-to-digital conversion with up to 4000/4096 angle steps
- Input frequencies: 500 kHz (x10), 80 kHz (x100), 8 kHz (x1000)
- Flexible pin assignment using signal path multiplexers
- PGA inputs for differential and single-ended signals
- Variable input resistance for current/voltage conversion
- Signal conditioning for offset, amplitude, and phase
- Controlled 50 mA current source for LED or MR sensor supply
- Fault-tolerant RS422 output via adjustable drivers (up to 50 mA)
- Glitch-free due to guaranteed minimum edge distance
- Index signal conditioning and electronic zero pulse generation
- Output of motor commutation signals: UVW with 1 to 8 cycles
- Signal and operation monitoring with a configurable alarm output, output shutdown and error storage
- I²C multi-master interface for configuration from ext. EEPROM
- I²C slave interface for in-circuit calibration and position data
- Adjustable over-temperature alarm and shutdown
- Supply from 4.3 to 5.5 V, operation from -40 to +100 °C
- Reverse-polarity-proof, including the sub-system

APPLICATIONS

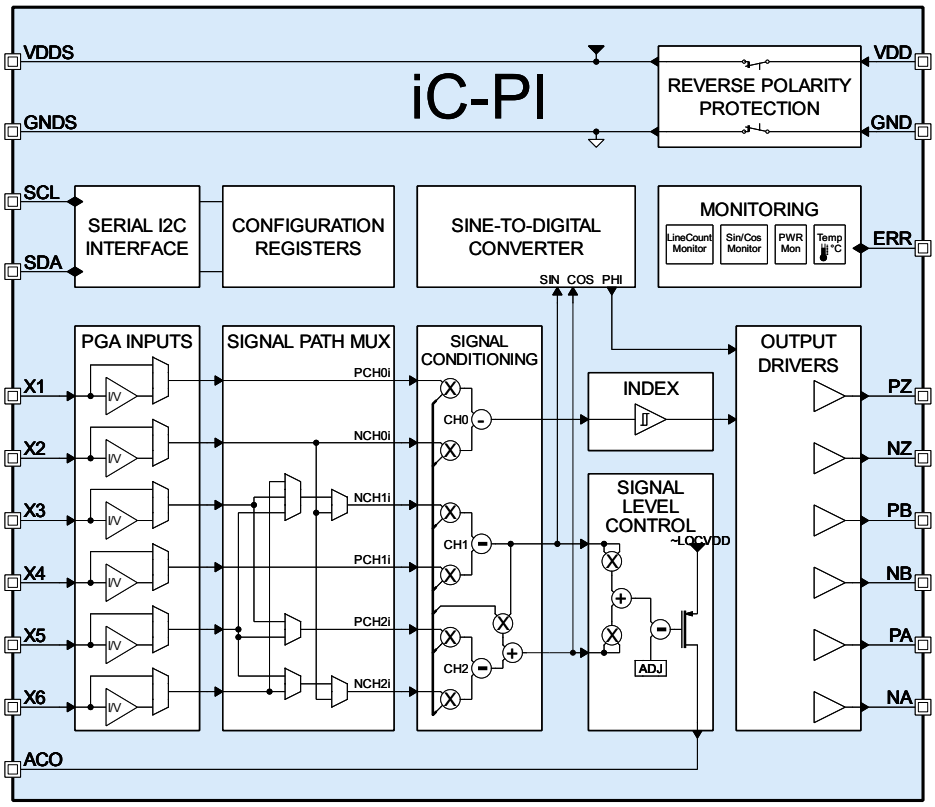
- Rotary and linear encoders
- Magnetic or optical angle sensor modules
- Brushless motor commutation

PACKAGES

TSSOP20

RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-PI is an interpolator with a non-linear A/D converter which digitizes sine/cosine sensor signals using a count-safe vector tracking conversion with both selectable resolution and hysteresis. The angle resolution per sine period can be set using SELRES; up to 4000 decimal angle steps, and up to 4096 binary angle steps are possible (see page 33).

The angle position is output incrementally by differential RS422 drivers as an encoder quadrature signal with a zero pulse or, if selected, as a counter signal for devices compatible with 74HC191 or 74HC193.

The zero pulse is generated electronically and output when the X1/X2 inputs receive an enable signal. This pulse can be configured extensively: both in its relative position to the input signal with regard to the logic gating with A and/or B and in its width from 90° to 360° (1/4 to 1 T).

A preselectable minimum edge distance ensures glitch-free output signals and prevents counting errors which in turn boosts the noise immunity of the position encoder.

Programmable instrumentation amplifiers with selectable gain levels allow differential or single-ended, referenced input signals; an external reference voltage can be connected to input X2 then operated as a reference input.

The modes of operation differentiate between high impedance (V modes) and low impedance (I modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected to the device. The optical scanning of low resolution code discs is also supported by the reference function of input X2; these discs do not evaluate tracks differentially but in comparison with a reference photodiode.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and any phase error between the sine and cosine signals to be corrected. The channel for the zero signal can be configured separately.

A control signal is generated from the conditioned signals which can track the transmitting LED of optical encoders via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage can also track the power supply of the measuring bridges. By tracking the sensor energy supply any temperature and aging effects are compensated for, the input signals stabilized and the exact calibration of the input signals is maintained. This enables a constant accuracy of the interpolation circuit across the entire operating temperature range.

If control limits are reached, these can be indicated at the maskable error pin ERR. Faults such as overdrive, wire breakage, short circuiting, dirt or aging, for example, can be logged.

iC-PI includes extensive self-test and system diagnosis functions which check whether the sensor is working properly or not. For all error events the user can select whether the fault is indicated at the pin ERR or whether the outputs should shutdown. At the same time errors can be stored in the EEPROM to enable failures to be diagnosed at a later stage. For encoder applications the line count of the code disc, the sensor signal regarding signal level and frequency and the operating temperature can be monitored, for example, the latter using an adjustable on-chip sensor.

Display error pin ERR is bidirectional; a system fault recognized externally can be recorded and also registered in the error memory.

iC-PI is protected against reverse polarity and offers its monitored supply voltage to the external circuit, thus extending the protection to the system (for load currents up to 20 mA). Reverse polarity protection also covers the short-circuit-proof output drivers so that an unintentional faulty wiring during initial operation is tolerated.
On being activated the device configuration is loaded via the serial I^2C interface from an external EEPROM and verified with a CRC. A microcontroller can also configure iC-PI; the implemented interface is multi-master-capable and allows direct RAM access to configuration and position data.

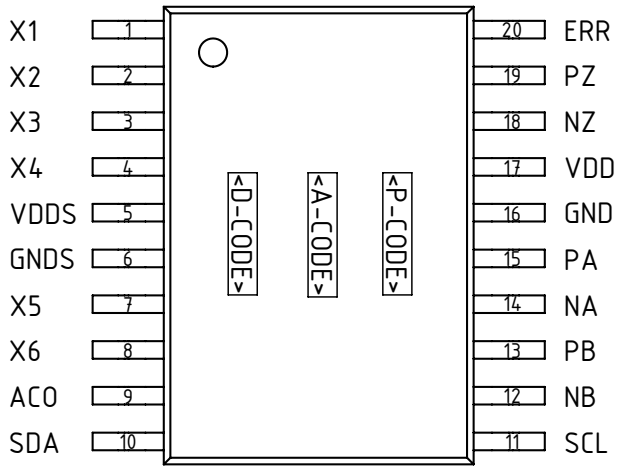
General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.
For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20



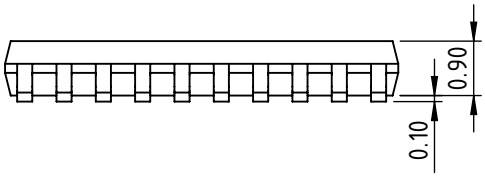
PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS[1]	Internal Analog Supply Voltage and Switched Supply Output (20 mA max.), reverse polarity proof
6	GNDS[1]	Switched Ground, reverse polarity proof
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Control, high-side current source output
10	SDA	Serial I^2C Interface, data line
11	SCL	Serial I^2C Interface, clock line
12	NB	Incr. Output B- / Commutation Outp. V
13	PB	Incr. Output B+
14	NA	Incr. Output A- / Commutation Outp. U
15	PA	Incr. Output A+
16	GND	Ground
17	VDD	+4.3...5.5 V Supply Voltage
18	NZ	Incr. Output Z- / Commutation Outp. W
19	PZ	Incr. Output Z+
20	ERR	Error Signal Input/Output

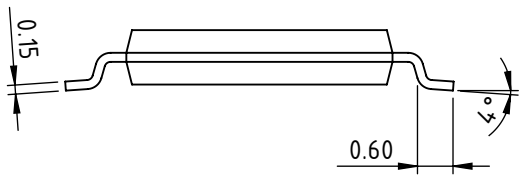
IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] It is advisable to connect a bypass capacitor of about 100 nF (up to 1 µF max.) close to the chip's analog supply terminals. If VDDS needs to provide more than 20 mA for the external circuitry, VDDS can be linked to VDD (same for GNDS to GND). However, whenever possible, analog and digital supplies should be separated to better filter the analog supply and maintain reverse polarity protection.

PACKAGE DIMENSIONS TSSOP20

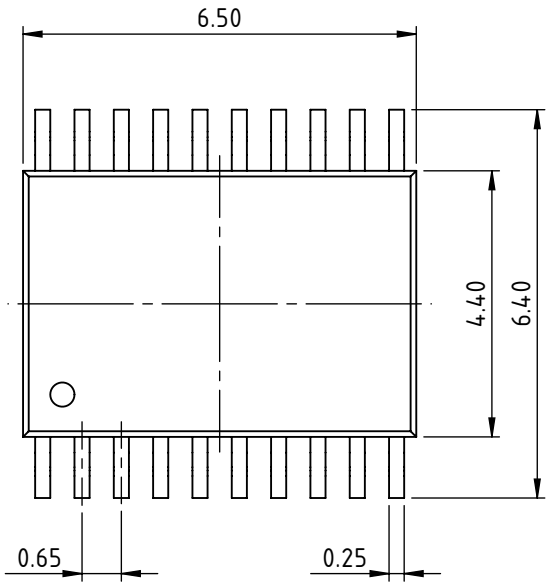
SIDE



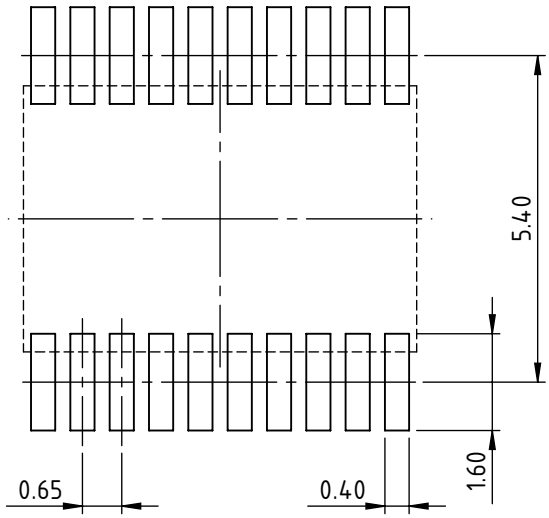
FRONT



TOP



RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, PA, NA, PB, NB, PZ, NZ, ACO	relative to GND if connecting VDDS to VDD, GNDS to GND	-6 0	6 6	V V
G002	V()	Voltage at ERR	relative to GND if connecting VDDS to VDD, GNDS to GND	-6 0	8 8	V V
G003	V()	Pin-to-Pin Voltage between VDD, GND, PA, NA, PB, NB, PZ, NZ, ACO, ERR			6	V
G004	V()	Voltage at VDDS	no reversed polarity at VDD and GND		VDD	V
G005	V()	Voltage at GNDS relative to GND	no reversed polarity at VDD and GND	-0.3	0.3	V
G006	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G007	I(VDD)	Current in VDD		-20	400	mA
G008	I()	Current in VDDS, GNDS		-50	50	mA
G009	I()	Current in X1...X6, SCL, SDA, ERR		-20	20	mA
G010	I()	Current in PA, NA, PB, NB, PZ, NZ		-150	150	mA
G011	I(ACO)	Current in ACO		-100	20	mA
G012	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G013	Ptot	Permissible Power Dissipation			300	mW
G014	Tj	Junction Temperature		-40	150	°C
G015	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		100	°C
T02	Rthja	Thermal Resistance Chip to Ambient			80		K/W

All voltages are referenced to pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Supply Voltage VDD versus GND	load current I(VDDS) up to 10 mA load current I(VDDS) up to 20 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current	Tj = -40...125 °C, no load Tj = 27 °C, no load		 28	35	mA mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vcz()hi	Clamp-Voltage hi at all pins				11	V
005	Vc()hi	Clamp-Voltage hi at Inputs SCL, SDA	Vc()hi = V() - V(VDDS), I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp-Voltage hi at Inputs X1...X6	Vc()hi = V() - V(VDDS), I() = 4 mA	0.3		1.2	V
007	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
008	Irev(VDD)	Reverse-Polarity Current VDD	V(VDD) = −5.5V...−4.3 V relative to GND			1	mA
PGA Inputs X1...X6 (i = 0 for CH0, i = 12 for CH1 and CH2)							
101	fin()	Permissible Maximum Input Frequency				500	kHz
102	Vin()sig	Permissible V-Mode Input Voltage Range	Ri() = 0x01 (V-Mode 1:1) BIAS12 = 1, Ri() = 0x09 (V-Mode 4:1) BIAS12 = 0, Ri() = 0x09 (V-Mode 4:1)	0.75 0 0		VDDS − 1.5 VDDS VDDS − 1.5	V V V
103	Vin()diff	Recommended Differential V-Mode Input Voltage	Vin()diff = V(PXi) − V(NXi); Ri() = 0x01 (V-Mode 1:1) Ri() = 0x09 (V-Mode 4:1)	 20 80		 500 2000	 mVpp mVpp
104	Vin()os	V-Mode Input Offset Voltage	relative to side of input, Ri() = 0x01; GRi and GFi = max. (max. gain)	-500		+500	µV
106	Iin()	V-Mode Input Current	Ri() = 0x01 (V-Mode 1:1)	-0.5		0.5	µA
107	Iin()sig	Permissible I-Mode Input Current Range	BIASi = 0, Ri(0) = 0 BIASi = 1, Ri(0) = 0	10 -300		300 -10	µA µA
108	Rin()	I-Mode / V-Mode Input Resistance	relative to VREFin, Tj = 27 °C Ri() = 0x00 Ri() = 0x02 Ri() = 0x04 Ri() = 0x06 Ri() = 0x09 (V-Mode 4:1)	 1.1 1.6 2.2 3.2 16	 1.7 2.5 3.5 4.9 20	 2.1 3.0 4.2 6.0 24	 kΩ kΩ kΩ kΩ kΩ
109	R2()	I-Mode Conversion Resistor	Tj = 27 °C; Ri() = 0x00 Ri() = 0x02 Ri() = 0x04 Ri() = 0x06 Ri() = 0x09 (V-Mode 4:1)		1.6 2.3 3.2 4.6 5.0		kΩ kΩ kΩ kΩ kΩ
110	TC(Rin)	Temperature Coefficient of Rin			0.15		%/K
111	Vin(X2)	Permissible Inp. Voltage $VREF_{ex}$ at X2 (during reference function)	MUX = 0x30...0x3F	0.5		VDDS − 2	V
112	Rin(X2)	Input Resistance at X2 (during reference function)	MUX = 0x30...0x3F, R0(3:0) = 0x01, R12(3:0) = 0x01 (all channels in V-Mode 1:1)	20	27	35	kΩ
113	C(X2)	Permissible C-Load at X2 (during output function)	MUX = 0x20...0x2F, I(X2) = -150...+150 µA			100	pF
114	Vout(X2)	Output Voltage at X2 (during output function)	MUX = 0x20...0x2F, relative to VREFin12; I(X2) = -10...+10 µA I(X2) = -150...+150 µA	 95 90	 100	 105 110	 % %
115	VREFI()	Internal Reference Voltages $VREFI_0$, $VREFI_{12}$	BIASi = 1 BIASi = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
116	Vt()hi	Input Threshold Hi at X1, X2 (during digital input mode)	DUAL = 1, R0 = 0x0, MUX(5:4) = 0			2	V
117	Vt()lo	Input Threshold Lo at X1, X2 (during digital input mode)	DUAL = 1, R0 = 0x0, MUX(5:4) = 0	0.8			V
118	Vt()hys	Input Hysteresis at X1, X2 (during digital input mode)	Vt()hys = Vt()hi - Vt()lo; DUAL = 1, R0 = 0x0, MUX(5:4) = 0	200			mV

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Conditioning CH0, CH1, CH2 (i = 0 for CH0, i = 12 for CH1 and CH2)							
201	G0, G12	Selectable Gain Factors	MODE = 0x05, Ri(3) = 0, GRi and GFi = 0x0 MODE = 0x05, Ri(3) = 0, GRi and GFi = max. MODE = 0x05, Ri(3) = 1, GRi and GFi = 0x0 MODE = 0x05, Ri(3) = 1, GRi and GFi = max.		6 300 1.5 75		
202	Gdiff	Relative Gain Ratio CH1 vs. CH2	GF2 = 0x10, GF1 = 0x0 GF2 = 0x10, GF1 = 0x7FF		39 255		% %
203	ΔG	Step Width Of Fine Gain Adjustment	for CH0 for CH1 for CH2		1.06 1.0009 1.06		
204	INL(Gi)	Integral Linearity Error of Gain Adjustment		-1.06		1.06	
205	VOScal	Offset Calibration Range	referenced to the selected source (VOS0 or VOS12), mode *Calibration 2*; ORi = 00 ORi = 01 ORi = 10 ORi = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
206	ΔOF0	CH0 Offset Calibration Step Width	referenced to the selected source VOS0; OR0 = 0x0		3.2		%
207	ΔOF12	CH1/2 Offset Calibration Step Width	referenced to the selected source VOS12; OR12 = 0x0		0.79		%
208	INL(OFi)	Integral Linearity Error of Offset Calibration	limited test coverage (guaranteed by design)	-5		5	LSB
209	PHI12	Phase Error Calibration Range	CH1 vs. CH2		±10.4		°
210	ΔPHI12	Phase Error Calibration Step Width			0.02		°
211	INL(PHI12)	Integral Linearity Error of Phase Calibration	limited test coverage (guaranteed by design)	-0.8		0.8	°
Sine-To-Digital Conversion							
301	fin()max	Maximum Permissible Input Frequency	refer to Figure 4 for dependencies; ABZ output at IPF x20, MTD = 0x00			500 390	kHz kHz
302	AAabs (INL)	Absolute Angle Accuracy (Integral Nonlinearity)	relative to input period (360 °), see Fig. 1, quasi-static input signal, ideal waveform, adjusted signal conditioning, w/o hysteresis error; any resolution (IPF x1 to x1024)	-0.2	± 0.13	+0.2	° °
303	AEhys	Systemic Absolute Angle Error With Hysteresis	see 302, refer to Fig. 2; SELHYS = 0x6 (1.0 °) SELHYS = 0x8 (2.0 °)		 0.5 1.0		 ° °
304	AArel (DNL)	Relative Angle Accuracy (Differential Nonlinearity)	relative to output period (T 100 %), see Fig. 3, quasi-static input signal, ideal waveform; IPF x1 IPF x50 IPF x125 IPF x250 IPF x500 IPF x1000 (4000 edges per period) IPF x1024 (4096 edges per period)		 1.7 3.5 7 14 28 28	 10 10 10 15 30 50 50	 % % % % % % %
305	ABrel	Relative Angle Accuracy A to B	see 302		1/2 AArel		%
306	AR	Repeatability	see 302 (w/o hysteresis error), VDD = const., Tj = const.		0.1		°
307	N	Output Angle Noise	see 302, 1 Vpp-diff sin/cos input, fin = 0 Hz			0.1	°
308	AEdiv	Systemic Relative Angle Error Using Subdivisions	relative to output period (T 100 %), see Fig. 3; any binary resolution any decimal resolution			 0 0	 % %

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output Drivers PA, NA, PB, NB, PZ, NZ							
501	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); SIK(1:0) = 00, I() = -1.2 mA SIK(1:0) = 01, I() = -4 mA SIK(1:0) = 10, I() = -20 mA SIK(1:0) = 11, I() = -50 mA			 200 200 400 700	 mV mV mV mV
502	Vs()lo	Saturation Voltage lo	SIK(1:0) = 00, I() = 1.2 mA SIK(1:0) = 01, I() = 4 mA SIK(1:0) = 10, I() = 20 mA SIK(1:0) = 11, I() = 50 mA			200 200 400 700	mV mV mV mV
503	Isc()hi	Short-Circuit Current hi	V() = 0 V; SIK(1:0) = 00 SIK(1:0) = 01 SIK(1:0) = 10 SIK(1:0) = 11	 -4 -12 -60 -150		 -1.2 -4 -20 -50	 mA mA mA mA
504	Isc()lo	Short-Circuit Current lo	V() = VDD; SIK(1:0) = 00 SIK(1:0) = 01 SIK(1:0) = 10 SIK(1:0) = 11	 1.2 4 20 50		 4 12 60 150	 mA mA mA mA
505	tr()	Rise Time	RL = 100 Ω to GND; SSR(1:0) = 00 SSR(1:0) = 01 SSR(1:0) = 10 SSR(1:0) = 11	 5 5 20 50		 20 40 140 350	 ns ns ns ns
506	tf()	Fall Time	RL = 100 Ω to VDD; SSR(1:0) = 00 SSR(1:0) = 01 SSR(1:0) = 10 SSR(1:0) = 11	 5 5 30 50		 20 40 140 350	 ns ns ns ns
507	Ilk()tri	Leakage Current	TRIHL(1:0) = 11 (tristate)		20	100	µA
508	Ilk()rev	Leakage Current	reversed supply voltage		100		µA
509	Rin()calib	Test Signal Source Impedance	mode *Calibration 1, 2, 3*: for any signal mode *TEST 5*: for signals PSIN, NSIN, PCOS, NCOS; fin() = TBD		2.5 2.5	4 4	kΩ kΩ
510	Rin()test5	Test Signal Source Impedance	mode *TEST 5*: for signals PZO, NZO; fin() = TBD	1			MΩ
511	I()cal	Permissible Test Signal Load	Op. modes *Calibration 1, 2, 3*	-3		3	µA
512	twhi	Duty Cycle at A, B	relative to output period T (see Fig. 1)		50		%
513	t_{AB}	Output Phase A to B	relative to output period T (see Fig. 1)		25		%
514	t_{MTD}	Minimum Edge Distance	See Fig. 1, system clock of 40 MHz; MTD = 0x0 MTD = 0x1	20 42	25 50	32 62	ns ns
515	Δt_{MTD}	Minimum Edge Distance Variation	VDD = 4.3...5.5 V, Tj = 27 °C, variation vs. VDD = 5 V, MTD = 0x01; VDD = 5 V, Tj = -40...125 °C, variation vs. Tj = 27 °C, MTD = 0x01;	-10 -5		+10 +15	% %
Signal Level Control, Current Source Output ACO							
601	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(), ACOT(1:0) = 0x2, ACOS(4:0) = 0x1F; ACOR(1:0) = 0x0, I() = -5 mA ACOR(1:0) = 0x1, I() = -10 mA ACOR(1:0) = 0x2, I() = -25 mA ACOR(1:0) = 0x3, I() = -50 mA			 1 1 1 1.2	 V V V V
602	Isc()hi	Short-Circuit Current hi	V() = 0 ... VDD - Vs()hi, ACOT(1:0) = 0x2, ACOS(4:0) = 0x1F; ACOR(1:0) = 0x0 ACOR(1:0) = 0x1 ACOR(1:0) = 0x2 ACOR(1:0) = 0x3	 -10 -20 -50 -100		 -5 -10 -25 -50	 mA mA mA mA
603	It()min	Control Range Monitoring 1: lower limit	refer to current range ACOR(1:0)		3		%Isc

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
604	It()max	Control Range Monitoring 2: upper limit	refer to current range ACOR(1:0)		90		%Isc
605	Vt()min	Signal Level Monitoring 1: lower limit	relative to Vscq()		40		%Vpp
606	Vt()max	Signal Level Monitoring 2: upper limit	relative to Vscq()		130		%Vpp
607	Vin(ACO)	Permissible Input Voltage for Offset-Tracking		0		VDDS	V
System Clock							
701	f()max	Max. Permissible System Clock Frequency				50	MHz
702	f()clk	System Clock Frequency	IBN calibrated to 200 µA IBN calibrated for 40 MHz (80 kHz at SCL)	28 34	37 40	49 50	MHz MHz
703	Δf()clk	System Clock Variation	VDD = 4.3...5.5 V, Tj = 27 °C, variation vs. VDD = 5 V; VDD = 5 V, Tj = -40...125 °C, variation vs. Tj = 27 °C;	-10 -5		10 15	% %
Bias Current Source and Reference Voltages							
801	IBN	Bias Current Source	*Calibration 1*, I(NB) vs. VDDS; CFGIBN = 0x0 CFGIBN = 0xF IBN calibrated at Tj = 25 °C	 110 180	 200	 370 220	 µA µA µA
802	VBG	Internal Bandgap Reference		1.18	1.25	1.32	V
803	VPAH	Reference Voltage		45	50	55	%VDDS
804	V05	Reference Voltage V05		450	500	550	mV
805	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold VDD, Power-Up-Enable	increasing voltage at VDD	3.6	4.0	4.3	V
902	VDDoff	Turn-off Threshold VDD, Power-Down-Reset	decreasing voltage at VDD	3.0	3.5	3.8	V
903	VDDhys	Hysteresis		0.4			V
Error Signal Input/Output, Pin ERR							
B01	Vs()lo	Saturation Voltage lo	versus GND, I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo	versus GND, V(ERR) ≤ VDD	4	5	8	mA
B03	Isc()	Low-Side Current Source For Data Output	versus GND, V(ERR) > VTMon L state Z state		 2 0		 mA mA
B04	Vt()hi	Input Threshold Voltage hi	versus GND			2	V
B05	Vt()lo	Input Threshold Voltage lo	versus GND	0.8			V
B06	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
B07	Ipu()	Input Pull-Up Current	V() = 0...VDD − 1 V, EPU = 1	-400	-300	-200	µA
B08	Vpu()	Pull-Up Voltage	Vpu() = VDD − V(), I() = -5 µA, EPU = 1			0.4	V
Reverse Polarity Protection and Supply Switches VDDS, GNDS							
C01	Vs()	Saturation Voltage vs. VDD	Vs(VDDS) = VDD − V(VDDS); I(VDDS) = -10...0 mA I(VDDS) = -20...-10 mA			 200 300	 mV mV
C02	Vs()	Saturation Voltage vs. GND	Vs(GNDS) = V(GNDS) − GND; I(GNDS) = 0...10 mA I(GNDS) = 10...20 mA			 200 250	 mV mV
C03	C()	Backup Capacitor Analog Supply VDDS vs. GNDS		100			nF

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3 ... 5.5 V, Tj = -40 °C ... 125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial I²C Interface SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	150	300		mV
D06	Ipu()	Input Pull-Up Current	V() = 0...VDDS – 1 V	-850	-300	-75	µA
D07	Vpu()	Pull-Up Voltage	Vpu() = VDDS – V(), I() = -5 µA			0.4	V
D08	fclk()	Clock Frequency at SCL	ENFAST = 0 ENFAST = 1	60 240	80 320	100 400	kHz kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibrated, EEPROM access without read failure, time to outputs operational; ENFAST = 0 ENFAST = 1		 36 24	 48 34	 ms ms
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated; V(SDA) = 0V V(SCL) = 0V or arbitration lost no EEPROM checksum ERROR		 4 indef. 45 95	 12 135 285	 ms ms ms ms
D11	tp()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant; IBN not calibrated IBN calibrated to 200 µA	 25 64	 80 80	 240 150	 µs µs
D12	fclk()ext	Permissible External Clock Frequency at SCL				400	kHz
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS – V(PA), *Calibration 3*, without load; Tj = -40 °C Tj = 27 °C Tj = 100 °C	 740 620 460	 770 650 520	 790 670 540	 mV mV mV
E02	TCs	Temp. Co. Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS - V(NA), Tj = 27 °C, *Calibration 3*, without load; CFGTA(3:0) = 0x0 CFGTA(3:0) = 0xF	 260 470	 310 550	 360 630	 mV mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Tw	Warning Temperature	CFGTA(3:0) = 0x0 CFGTA(3:0) = 0xF	125	140 65	 80	°C °C
E06	Thys	Warning Temperature Hysteresis	80 °C < Tj < 125 °C	10	15	25	°C
E07	ΔT	Relative Shutdown Temperature	ΔT = Toff – Tw	5	15	25	°C

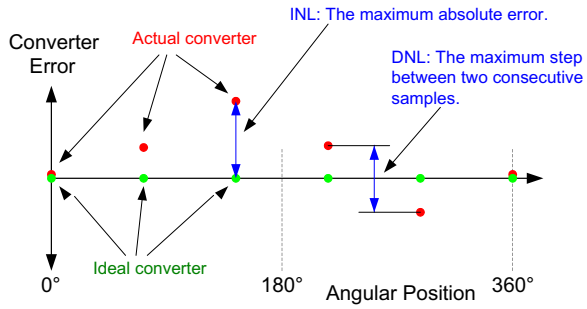


Figure 1: Integral and differential nonlinearity.

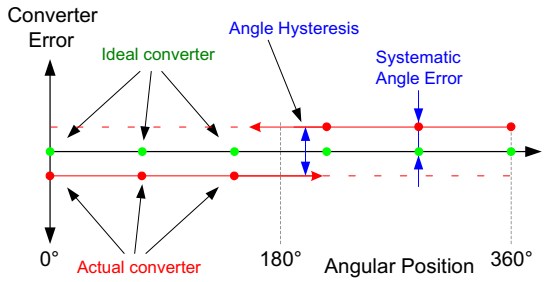


Figure 2: Systematic angle error due to hysteresis.

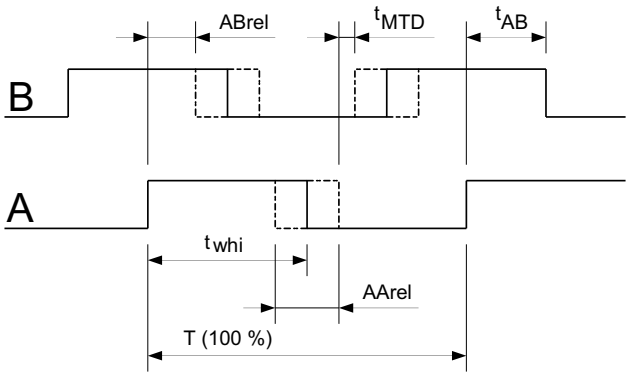


Figure 3: Relative angle error and minimum edge distance.

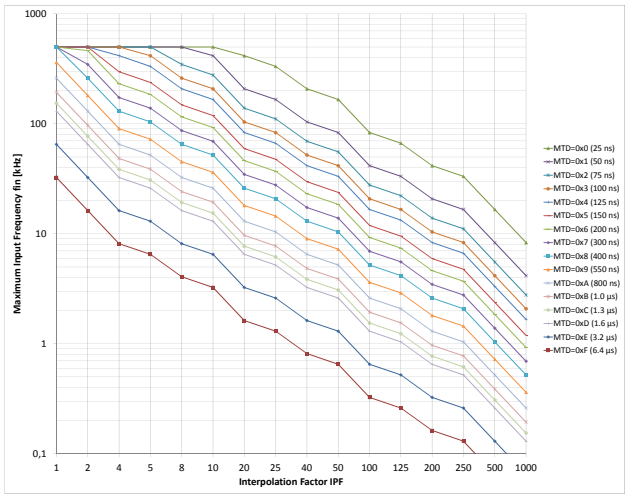


Figure 4: Maximum input frequency depending on interpolation factor. See also Table 43, page 33.

PROGRAMMING

CONFIGURATION REGISTERS

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Calibration								
0x00	0	0	0	ENFAST	CFGIBN(3:0)			
0x01	0	0	0	0	CFGTA(3:0)			
Operating Mode								
0x02	RUN	ENSL	0	ENZFF	MODE(3:0)			
Input Configuration								
0x03	ENF	MUX(6:0)						
0x04	0	BIAS0	VOS0(1:0)		R0(3:0)			
0x05	0	BIAS12	VOS12(1:0)		R12(3:0)			
0x06*	1	1	0	1	0	0	0	0
Signal Conditioning CH0								
0x07	DUAL	GR0(2:0)			0	0	OR0(1:0)	
0x08	0	0	0	GF0(4:0)				
0x09	0	0	OF0(5:0)					
Signal Conditioning CH1, CH2								
0x0A	GF1(3:0)				0	GR12(2:0)		
0x0B	0	GF1(10:4)						
0x0C	0	0	0	GF2(4:0)				
0x0D	MP1(7:0)							
0x0E	MP2(3:0)				0	0	MP1(9:8)	
0x0F	0	0	MP2(9:4)					
0x10	OF1(3:0)				OR2(1:0)		OR1(1:0)	
0x11	0	OF1(10:4)						
0x12	OF2(7:0)							
0x13	PH12(3:0)				0	OF2(10:8)		
0x14	0	0	PH12(9:4)					
Signal Level Control								
0x15	ACOR(1:0)		ACOS(4:0)					0
0x16	0	ACOHYS(2:0)			0	0	ACOT(1:0)	
Error Monitoring and Alarm Output								
0x17	EMASKA(7:0)							
0x18	0	EMTD(2:0)			0	0	EMASKA(9:8)	
0x19	EMASKO(7:0)							
0x1A	0	PDMODE	EPU	EPH	0	0	EMASKO(9:8)	
0x1B	EMASKE(7:0)							
0x1C	0	0	0	0	0	0	EMASKE(9:8)	
Zero Signal Output								
0x1D	CFGABZ(7:0)							
0x1E	CFGZPOS(7:0)							
Sine-To-Digital-Conversion, Minimum Edge Distance								
0x1F	MTD(3:0)				SELHYS(3:0)			
0x20	SELRES(7:0)							
0x21	0	0	HOLDCNT	STUPCNT	SELRES(11:8)			

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Output Driver Settings								
0x22	0	0	SIK(1:0)		SSR(1:0)		TRIHL(1:0)	
Line Counter								
0x23	LINECNT(7:0)							
0x24	0	0	LINECNT(13:8)					
Sine-To-Digital-Conversion, Calibration, Commutation								
0x25	0	POLES(2:0)			0	0	0	0
Reserved								
0x26	OFFSET(7:0)							
0x27	0	0	0	0	0	0	0	0
0x28	0	0	0	0	0	0	0	0
0x29	free for OEM data							
0x2A	free for OEM data							
0x2B	free for OEM data							
0x2C	free for OEM data							
0x2D	free for OEM data							
0x2E	free for OEM data							
Checksum								
0x2F	CHKSUM(7:0)							
Error Register								
0x30	ERRFIRST(7:0)							
0x31	ERRACT(5:0)						ERRFIRST(9:8)	
0x32	ERRACC(3:0)				ERRACT(9:6)			
0x33	0	0	ERRACC(9:4)					
Position Data								
0x34	SENSDAT(11:4)							
0x35	SENSDAT(3:0)				XD		ESYNC	EINC
0x36	PMODE	PERIOD(14:8)						
0x37	PERIOD(7:0)							
0x3F	CHPREL(7:0), refer to Table 8							
Notes	The device RAM initially contains random data following power-on. On a voltage drop below the Power Down Reset Threshold VDDoff (Elec. Char. 902), the configuration is refreshed from the connected EEPROM. If there is no EEPROM and the IC is operated via I2C, the external MCU must check or refresh the configuration (just registers 0x00 to 0x02, and 0x15 to 0x1C will be zeroed automatically). In general, unused register bits must be programmed to zero unless otherwise noted. *) Programming to 0xD0 is required and mandatory for regular operation.							

Table 1: Register Layout (EEPROM)

SERIAL I²C INTERFACE

The multi-master capable I²C interface consists of two bidirectional pins, SCL (for clock) and SDA (for data), and enables iC-PI to restore its configuration from the external serial EEPROM. For this function, the readout can be accelerated from ENFAST reading onwards if a higher clock frequency is selected as an option.

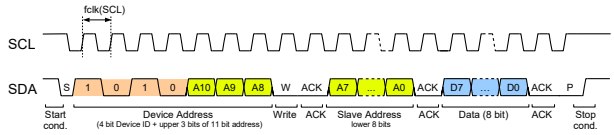


Figure 5: I²C slave addressing for writing a single byte to the EEPROM.

Furthermore, the I²C interface can be enabled to operate as an I²C slave (using ENSL), allowing an external I²C master to read iC-PI's position data, as well as edit its configuration data.

ENFAST	Addr. 0x00, bit 4
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors (e.g. 2.2 kΩ for line capacitances of up to 170 pF and clock rate 320 kHz; the permissible minimum value is 1.5 kΩ). A ground trace between SCL and SDA is recommended to avoid cross talk.

Table 2: I²C Fast Mode

ENSL	Addr. 0x02, bit 6
Code	Function
0	I²C slave mode disabled
1	I²C slave mode enabled (Device ID 0x55)

Table 3: I²C Slave Mode

I²C Master Performance	
Protocol	Standard I²C
Output Clock Rate	100 kHz max. (see Elec.Char. D08), 400 kHz max. using ENFAST = 1
Addressing	11 bit: 8 bit register address plus 3 bit block selection
Access Trials	Read: up to 4x at power-on (I²C error: acknowledge missing), 1x at byte reading, 1x at byte writing (for consecutive writing with pauses from byte to byte)
Multi-Master Capability	Yes
I²C Slave Performance	
Input Clock Rate	400 kHz max. (see Elec.Char. D12)
Device ID	0x55 ('1010 101' w/o R/W bit)

Table 4: I²C interface performance

Note: The I²C bus lines are sensitive. Keeping the traces short and shielding them with ground prevents unwanted actions.
The use of pull-up resistors (e.g. 2.2 kΩ at SCL and SDA) supports the bus signals on logic high and improves the EMI immunity.

Note: When programming the EEPROM in-circuit, iC-PI must be powered up in advance.
Note that power must be maintained (e.g. for 10 ms) to allow the EEPROM finishing its write operation.

Attention: If a power failure interrupts the EEPROM's write operation, the entire page content may be lost.

Attention: If error logging is enabled and periodic errors occur (e.g. 1 event/turn), the maximum permissible write cycles may be exceeded.
Thus, the recommended precaution is to disable error logging (refer to EMASKE), and to lock the EEPROM by its WP pin after factory calibration.

EEPROM Device Requirements

EEPROM Device Requirements	
Supply Voltage	3.3 V to 5.5 V
Power-On Threshold	< 3.3 V (due to Elec.Char. 901)
Addressing	11 bit address max.
Device ID	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Support of *Page Write* with pages of at least 4 bytes.
Size Minimum	512 bit (64x8 bit) (address range used is 0x00 to 0x3F)
Size Maximum	8 Kbit (4x 256x8 bit), type 24C08

Table 5: EEPROM Device Requirements

If the EEPROM does not feature *Page Write*, error events can not be saved (EMASKE must be configured to 0x00).

The following EEPROMs have been recommended, but may need to be re-tested for the above conditions: Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W.

Attention: EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB) should not be used with the iC-PI.
EEPROMs that use the address pins as additional enable bits should be used instead.

Attention: When I²C Slave Mode is enabled, iC-PI responds to device ID 0x55, limiting the maximum EEPROM size to 8 Kbit (0x50 to 0x53 addresses 4x 256 bytes).

Device Startup

Once the supply has been switched on, the iC-PI outputs are high impedance (tristate) until a valid configuration is read from the EEPROM using device ID 0x50.

If the configuration data is not confirmed by its checksum, the readin process is repeated. If no valid configuration data is available after a fourth attempt, iC-PI terminates communication with the EEPROM and enables I²C slave mode. For timing information, refer to the Electrical Characteristics, items D10 and D11.

For devices loading a valid configuration from the EEPROM, bit ENSL defines whether the I²C slave function is enabled or not.

Configuration Data Checksum

The checksum at address 0x2F is used to initially confirm the configuration data read from the EEPROM, as well as to permanently monitor the configuration data in the RAM during operation. Detecting a bit flip can take half a millisecond, approximately.

CHKSUM	Addr. 0x2F, bit 7:0
Code	Function
0x00... ...0xFF	Checksum for address range 0x00 to 0x2E; CRC polynomial 0x11D ($x^8 + x^4 + x^3 + x^2 + 1$) Start value: 0x01

Table 6: Configuration Data Checksum

Example of CRC calculation routine:

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

I²C Slave Mode (ENSL = 1)

In this mode iC-PI behaves like an I²C slave with the device ID 0x55 and the I²C interface permits iC-PI's internal registers to be read and written. An I²C start condition (S) is indicated by a falling edge on SDA while SCL remains high. This initiates the I²C sequence and prevents other masters from driving the bus. Next, the iC-PI device ID (0x55) must be written by the master followed by the read/write mode bit (W). A low W bit selects write mode and a high W bit selects read mode. iC-PI acknowledges the valid device ID by pulling SDA low while the master is not driving SDA (A).

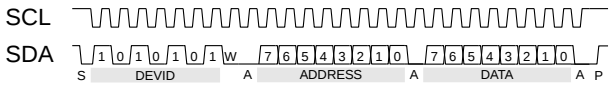


Figure 6: I²C write command in slave mode

The next 8 bits are the iC-PI address at which the data is to be written. After the 8th bit, iC-PI again acknowledges the received bits by pulling SDA low after a falling edge on SCL. The third and following bytes contain the data to be written. After a byte has been written, the address is incremented so that multiple bytes can be written sequentially *.
If the address is valid, the iC-PI acknowledges the write command. After the last byte, the master must release SCL so it is pulled high and then also release SDA to generate a stop condition (P).

For reading a register via I²C interface, the desired register address must be sent to the iC-PI via an I²C write command. After the address is acknowledged by iC-PI, the master has to restart (R) the I²C sequence by placing a second start edge on SDA with SCL remaining high. Next, the read command begins with the DEVICE ID and the read/write mode bit (W) set to select read mode (high).

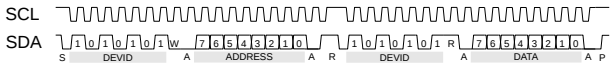


Figure 7: I²C read command in slave mode

If the address is valid, the iC-PI acknowledges the register read by pulling SDA low (A) and then transmits the register contents of the specified address. After a byte is read, the address is incremented so that multiple bytes can be read sequentially. After each byte, the master has to acknowledge that the byte was received by pulling SDA low. Otherwise the iC-PI goes into I²C idle mode.

Figure 8 shows a read request of position data at addresses 0x34 and 0x35, and the latch event of the sensor data.

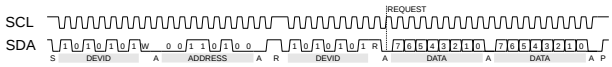


Figure 8: I²C position data read command in slave mode

Device Configuration Using I²C Slave Mode

The registers 0x00 to 0x2E must be initialized with correct values before enabling iC-PI. This can be done through the I²C slave interface if iC-PI is used without an EEPROM or if the EEPROM content is invalid. Initially, RUN (bit 7 of address 0x02) must be set to zero, then all registers must be configured. Finally, set RUN to one without changing other bits of address 0x02 to enable the device.

RUN	Addr. 0x02, bit 7
Code	Function
0	Device standby: Sin/D converter disabled, all output drivers show low (configuration changes allowed, see Table 10)
1	Device enabled: Restart of Sin/D conversion, state of output drivers depends on error conditions (tristate on temperature or configuration/checksum error; state halted on loss of signal (for HOLDCNT = 1, see Table 46, page 33)
Notes	RUN is evaluated only during I²C slave mode. Writing changes the function. Reading does not return the chip's state.

Table 7: Device Enable

If an EEPROM is connected and iC-PI is enabled for error logging (refer to description on page 40), the error memory needs to be cleared afterwards.

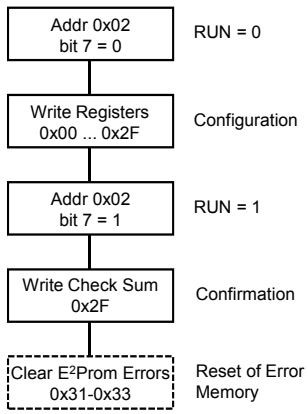


Figure 9: Programming via I²C. RUN is altered by changing only bit 7 of address 0x02 and leaving bits 6:0 unchanged.

* Regarding the availability of sequential write, refer to the design review on page 48.

Note: iC-PI verifies its RAM contents cyclically versus the checksum stored at address 0x2F. As these check cycles take less than half a millisecond, writing a single byte or parameter can trigger a configuration error, at least temporarily, until the checksum has been updated.

Note: When finally clearing the error memory, the sensor system should run properly as otherwise iC-PI may update the error memory immediately (if error logging is enabled).

Identification of Chip Release

For chip release verification purposes an identification value is stored at address 0x3F; writing to this ROM address is not permitted.

CHPREL	Addr. 0x3F, bit 7:0 (ROM)
Code	Chip Release
0x34	iC-PI Y
0x35	iC-PI Y1
0x36	iC-PI X

Table 8: Chip Release

Access Rights

Register	Read access in I²C slave mode (ENSL = 1)
RAM Addr.	Content
0x00-0x2F	Configuration data (see EEPROM addresses 0x00-0x2F)
0x30-0x33	Error data (see EEPROM addresses 0x30-0x33)
0x34-0x37	Position data
0x38-0x3E	Not available
0x3F	Chip release CHPREL(7:0)
0x40-0x7F	Not available

Table 9: RAM Read Access

The internally available absolute angle information can be accessed by reading addresses 0x34 and 0x35. Each time address 0x34 is read the internal position data is latched.

Register	Write access in I²C slave mode (ENSL = 1)
RAM Addr.	Access and conditions
0x00-0x1C	Changes permitted, no restrictions
0x1D-0x25	Changes permitted during standby (RUN = 0)
0x26-0x2F	Changes permitted, no restrictions
0x30-0x33	Changes permitted, no restrictions
0x34-0x35	No write access permitted
0x36	Write access impacts bit 7 (PMODE) only.
0x37-0x3F	No write access permitted

Table 10: RAM Write Access

POSITION DATA OUTPUT USING I²C

SENSDAT	Addr. 0x34-0x35	
Addr.	Bits	Function
0x34 [1]	7:0	Sensor Data 11:4 [2]
0x35	7:4	Sensor Data 3:0 [2]
0x35	3	Pin X2 state [3]
0x35	2	Pin X1 state [3]
0x35	1	ESYNC: Synchronization Error [4]
0x35	0	EINC: Incremental Error [5]
Notes	[1] Accessing 0x34 latches the position registers 0x34...0x37 for consistent position data (using PDMODE = 0). Accessing 0x34 also latches the error states of EMASK to output ESYNC and EINC. [2] The zero angle follows the zero position configured by CFGZPOS. [3] Status of digital input pin (using DUAL = 1). [4] ESYNC corresponds to error bit 7 from EMASKA: Excessive Input Frequency. [5] EINC corresponds to error bit 8 from EMASKA: Excessive Output Lag.	

Table 11: Position Data: Angle

PERIOD	Addr. 0x36-0x37	
Addr.	Bits	Function
0x36 [4]	7	PMODE: Period Counting Mode
0x36	6:0	Period high
0x37	7:0	Period low
Notes	[4] Accessing 0x36 latches 0x36 and 0x37 for consistent period data (using PDMODE = 1).	

Table 12: Position Data: Period

By reading address 0x34, the internal single-turn position (register sensor data) and multiturn position (register period data) are latched, so that the position data can be accessed by a burst read from address 0x34 to 0x37.

If the period counting mode PMODE is configured to 0, the current period count of full sine-periods is presented by the period registers. When passing the index mark in the positive direction, the register's value is cleared to zero; when passing in the negative direction the signed register's value becomes negative.

If the period counting mode PMODE is configured to 1, the last period count between the last two consecutive index signals is presented by the period registers. This feature can be used with distance-coded index marks. When moving in the positive direction, the MSB (sign bit) is 0 and when moving in the negative direction, the MSB is 1. The lower bits represent the unsigned number of periods. The period register's content is zero initially, until two consecutive index signals have passed in the same moving direction.

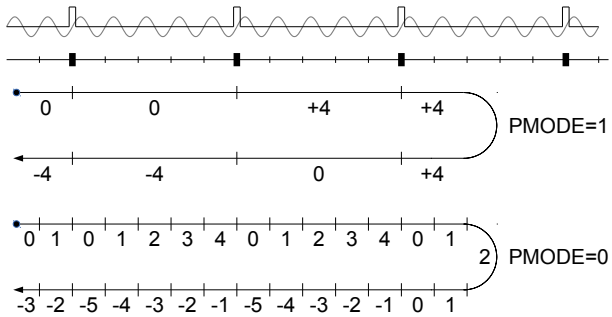


Figure 10: Output of PERIOD register in PMODE 0 and 1 with index pulse every 5 periods

PMODE	Addr. 0x36, bit 7
Code	Function
0	Current counted periods
1	Last counted periods

Table 13: Period Counting Mode

BIAS CURRENT SOURCE AND TEMPERATURE SENSOR

Bias Current Calibration

The calibration of the bias current source in operation mode *Calibration 1* (refer to Table 16 for an overview of operating modes) is required to adhere to the given Electrical Characteristics and also instrumental in the determination of the chip timing (e.g. clock frequency at SCL).

The IBN bias current is measured by connecting **pin VDDS** and **pin NB** with a 10 kΩ resistor. When the voltage drop is 2 V, the bias current is adjusted to its target value of 200 µA.

CFGIBN	Addr. 0x00, bit 3:0		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 14: Bias Current

Temperature Sensor Calibration

The temperature monitoring is calibrated in operating mode *Calibration 3* (refer to Table 16 for an overview of operating modes).

The following settings are required for this measurement: EMASKA = 0x20 (excessive temperature warning enabled), EMTD = 0x00 (shortest alarm indication time), and EPH = 0x00 (alarm output active low).

First, the temperature sensor voltage at which the warning message is generated, VTs, must be determined. A voltage ramp from VDDS towards GNDS is applied to pin PA until pin ERR pulls low (at approx. 4.4 V when coming from 5.0 V).

Note that the signal at pin ERR switches from tristate to low (on reaching VTs) and already at just 25 mV lower from low to tristate (on overshooting the temperature shutdown threshold, which is not relevant to calibration). To avoid confusion, a clear change of state (from high → low → high) should be generated using an external pull-up resistor at pin ERR.

Example: $VTs(T_1)$ is approx. 640 mV, measured from VDDS versus PA, with T_1 = 25 °C;

The necessary warning activation threshold, $VTth(T_1)$, is then calculated. The required warning temperature T_2, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E), and measurement value $VTs(T_1)$ are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: for $T_2 = T_1$ + 100 K $VTth(T_1)$ must be programmed to 434 mV.

Reference voltage $VTth(T_1)$ is provided for a high impedance measurement (10 MΩ) at output pin NA (measurement against VDDS) and must be set to the calculated value by programming CFGTA(3:0).

Example: altering $VTth(T_1)$ from 315 mV (measured with CFGTA(3:0)= 0x0) to 434 mV is equivalent to 138 %, the closest value for CFGTA is 0x8;

CFGTA	Addr. 0x01, bit 3:0		
Code k	$VTth \sim \frac{65+3.25k}{65}$	Code k	$VTth \sim \frac{65+3.25k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	CFGTA = 0xC: Tw is approx. 85 °C, and Toff is approx. 97 °C typically. CFGTA = 0x8: Tw is approx. 125 °C, and Toff is approx. 137 °C typically.		

Table 15: Temperature Monitoring

OPERATING MODES

The iC-PI has several operating modes, for which the functions of outputs PA, NA, PB, NB, PZ, NZ and ERR are different.

Three operating modes are available for the output of the angle position in normal operation. Mode 191/193 provides control signals for devices compatible with 74HC191 or 74HC193. Mode ABZ provides incremental position as encoder quadrature signals with a zero pulse. Mode UVW provides both incremental encoder quadrature (ABZ) and commutation outputs as single-ended signals. Only in these modes are the line drivers and the reverse polarity protection feature active.

In order to condition the input signals and to calibrate and test the iC-PI, various Calibration and Test modes are also available. Digital and analog test signals are provided; the latter must always be measured at high load impedance. The output drivers and the reverse polarity protection feature are not active during Calibration and Test modes.

MODE(3:0)		Addr. 0x02; bit 3:0						
Code	Operating Mode	Pin PA	Pin NA	Pin PB	Pin NB	Pin PZ	Pin NZ	Pin ERR
0x00	ABZ	A+	A-	B+	B-	Z+	Z-	ERR/ Z_{In}**
0x0E	UVW	A+	U	B+	V	Z+	W	ERR
0x0F	191/193	CPD	CPU	CP	nU/D	MR	nPL	ERR
0x01	Calibration 1	res.	res.	res.	IBN	PCH0	NCH0	res.
0x02	Calibration 2	PCH1	NCH1	PCH2	NCH2	VDC1	VDC2	res.
0x03	res. *	res.	res.	res.	res.	res.	res.	res.
0x04	res. *	res.	res.	res.	res.	res.	res.	res.
0x05	Test 5	PSIN	NSIN	PCOS	NCOS	PZO	NZO	IERR
0x06	Test 6 (MUX=0x40)	X4	X6	X3	X5	X1	X2	res.
0x07	Calibration 3	VTs	VTth	res.	res.	VTTFE	VTTSE	ERR
0x08	res. *	res.						
0x09	res. *	res.						
0x0A	res. *	res.	res.	res.	res.	res.	res.	res.
0x0B	System Test ***	A_8	A_4	B_8	B_4	Z_{In}	TP1	ERR
0x0C	res. *	res.	res.	res.	res.	res.	res.	res.
0x0D	res. *	res.	res.	res.	res.	res.	res.	res.
	Hints	*) Test function for iC-Haus device test only. **) Requires EMASKA = 0x010 and EMTD = 0x00. ***) Using System Test, the input frequency may not exceed 1 kHz.						

Table 16: Operating Modes

ABZ Mode
The angle position is output incrementally as encoder quadrature signals with a zero pulse. All output drivers are active and output complementary RS422-compatible signals at PA and NA, PB and NB, and PZ and NZ. The P prefix indicates a positive-going signal, the N prefix an inverted and negative-going signal.

UVW Mode
This mode outputs encoder quadrature signals and brushless motor commutation signals. All output drivers are active and output single-ended signals for A, B, Z (at the Px pins), and U, V, W (at the Nx pins).

191/193 Mode

In this mode the outputs provide control signals for counter devices compatible with 74HC191 or 74HC193 according to the following table. When the output drivers are active, the driving capability (SIK) and the driver's slew rate (SSR) must be adjusted so that the clock pulses can be output with a short low pulse according to the chosen minimum edge distance (see Page 38).

191/193 Mode		
Pin	Signal	Description
PA	CPD	Clock Down Pulse
NA	CPU	Clock Up Pulse
PB	CP	Clock Pulse
NB	nU/D	Count Direction (0: up, 1: down)
PZ	MR	Asynch. Master Reset (active high) Signal is '1' if index position is reached, otherwise '0'.
NZ	nPL	Asynch. Parallel Load Input (active low) / Reset (active low) Signal is '0' if index position is reached, otherwise '1'.

Table 17: Description of pin signals in 191/193 Mode (for 74HC191, 74HC193 and compatible devices).

Calibration Modes 1, 2, 3

In mode *Calibration 1* the IBN bias current (at pin NB) and the analog signals PCH0 and NCH0 of the zero channel can be measured (at pin PZ and NZ). Refer to page 21 for the calibration of the IBN bias current, and to page 29 for the calibration of the zero channel.

In mode *Calibration 2* the conditioned sine and cosine signals are output (PCH1, NCH1 and PCH2, NCH2). These signals are supplied at a lower gain, which is reduced by a factor of 6. The VDC offset references VDC1 and VDC2 are also provided at the pins PZ and NZ (relevant when VOS12 = 0x3). For a description of the calibration process, see page 27.

In mode *Calibration 3* the internal temperature monitoring signals are provided. Refer to page 21 for a description of the calibration of temperature monitoring.

Test Mode 5

In mode *Test 5* the conditioned sine and cosine signals (PSIN, NSIN, PCOS, NCOS) and the conditioned zero signal (PZO, NZO) are output. These sine and cosine signals are the signals which are evaluated by the sine-to-digital converter section; their amplitude is 6-fold the output level in mode *Calibration 2*. The zero signal output level is the same as in mode *Calibration 1*.

Test Mode 6

The input voltages at the pins X3 to X6 can be checked in mode *Test 6*. The following settings are required:

- MUX = 0x40

System Test Mode and Digital Calibration

This mode allows the signal conditioning to be adjusted. At a resolution of 4, the interpolator generates an encoder edge every 90 degrees. At a resolution of 8, the interpolator generates an encoder edge every 45 degrees. The objective of the calibration procedure is an output duty cycle of exactly 50 % for A_4, B_4, A_8, and B_8.

System Test		
Pin	Signal	Description
PA	A_8	Phase deviation from 90° between CH1 and CH2
NA	A_4	Offset CH1
PB	B_8	Amplitude deviation between CH1 and CH2
NB	B_4	Offset CH2
PZ	Z_{ln}	Digital zero signal, unmasked
NZ	TP1	Verification of line count (pulses) between two zero pulses Low signal: verification running (state after power on reset) High signal: verification finished An error messaging at ERR is valid after the second zero signal (enable required).
The following settings are required for mode *System Test*: MODE = 0x0B, SELRES = 0x0007, SELHYS = 0xF, CFGABZ(7:4) = '0000'; Note that the input frequency may not exceed 1 kHz.		

Table 18: Digital Calibration Signals

PGA INPUT CONFIGURATION AND SIGNAL PATH MULTIPLEXER

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Single-ended input signals can be processed by applying the input signal's reference voltage to the negative inputs, and to X2, when using the single-ended input configuration.

Both voltage and current signals can be accepted as input signals. For selection, use registers R12 and R0.

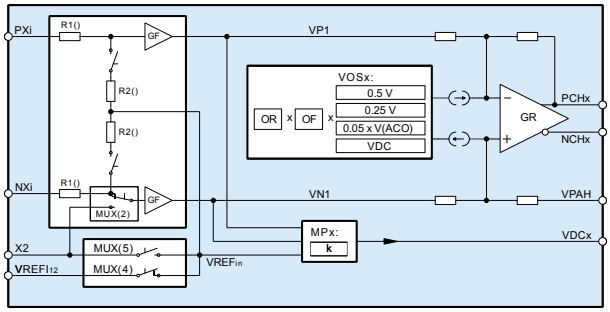


Figure 11: Signal conditioning input circuit.

Voltage Signals

In voltage mode (V-Mode), an optional voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to 25 % of the original. The internal circuit corresponds to the circuit in current mode, just the in-line resistor R1 is altered.

Current Signals

In current mode (I-Mode), an internal resistor R2() becomes active at each input, converting the current signal into a voltage signal. The effective input resistance Rin() is always determined by the sum of R1 and R2, whereas R2 is linking to the selectable reference voltage VREFin.
R2 should be set to obtain approx. 125 mV to 250 mV for the VDC offset references (for VDC1 and VDC2, using operating mode Calibration 2).

Note: The input circuit is not suitable for back-to-back photodiodes.

R12	Addr. 0x05, bit 3:0		
R0	Addr. 0x04, bit 3:0		
Code	In-line R1()	Internal R2()	I/V Mode
x000	0.1 kΩ	1.6 kΩ	I-Mode
x010	0.2 kΩ	2.3 kΩ	I-Mode
x100	0.3 kΩ	3.2 kΩ	I-Mode
x110	0.3 kΩ	4.6 kΩ	I-Mode
0xx1	3.5 kΩ	High impedance	V-Mode 1:1
1xx1	15 kΩ	5 kΩ	V-Mode 4:1°
Notes	Nominal values; Rin = R1() + R2(); for tolerances refer to Elec.Char. No. 108, 109, and 110. VREFin is the voltage divider's footpoint. Input currents may be positive or negative (Vin > VREFin, or Vin < VREFin). When using X2 as reference and single-ended input configuration, use R12 = R0. *) Refer to Elec. Char. No. 102 for permissible input voltage range.		

Table 19: I/V Mode and Input Resistance

Input Reference Voltages

The parameters BIAS12 and BIAS0 determine the input circuit's internal reference voltages $VREFI_{12}$ and $VREFI_0$.

BIAS12	Addr. 0x05, bit 6
BIAS0	Addr. 0x04, bit 6
Code	Function
0	VREFI = 2.5 V for low-side current sinks (e.g. photodiodes with common anode at GNDS) **Note*:** V(PXi) + V(NXi) < 2 x VREFin
1	VREFI = 1.5 V for high-side currrent-sources (e.g. photodiodes with common cathode at VDDS) for voltage sources relative to ground (e.g. iC-SM2, Wheatstone sensor bridges) for voltage sources with low-side reference (e.g. iC-LSHB, when using MUX(5:4) = 3) **Note*:** V(PXi) + V(NXi) > 2 x VREFin
Notes	*) Condition is relevant only if using - the VDC offset references (see Table 25) - the input voltage divider (see Table 19) - sum control mode (see Table 37)

Table 20: Reference Voltage

In the generation of the VDC offset references, BIAS12 also determines whether the reference voltage VREFin is subtracted from the sum of the particular input signals or the sum is subtracted from VREFin.

In the generation of the VDC offset references it is also essential that the input circuit refers to the same footpoint as the incoming sensor signals.

For footpoint levels above ground, MUX(5:4) = 0x3 allows to replace both internal $VREFI_{12}$ and $VREFI_0$ sources by the sensor's reference voltage, connected as $VREF_{ex}$ to input X2.

Vice versa, using MUX(5:4) = 0x2, iC-PI's internal $VREFI_{12}$ can be output to X2, to be used as reference for the external sensor circuit (using an opamp for buffering is required).

Note that whenever X2 is used to output $VREFI_{12}$, or to input $VREFI_{ex}$ from an external reference, $VREFI_{in}$ is always the same for CH1, CH2, and CH0.

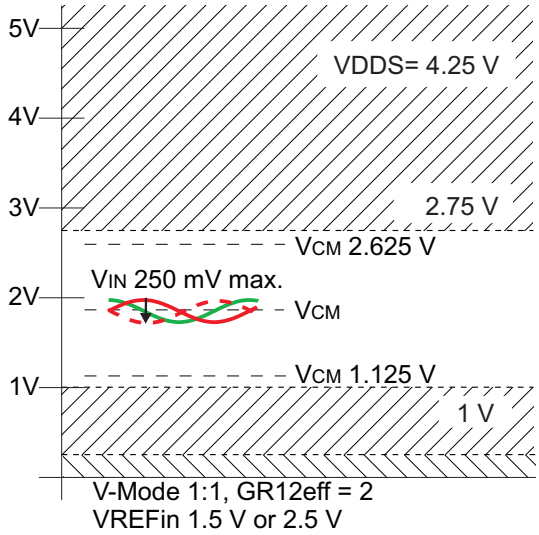


Figure 12: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G12_{eff}$ = 2.0 and V-Mode 1:1

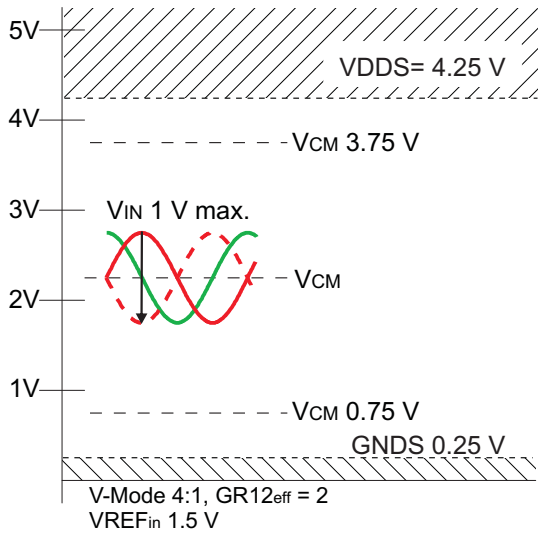
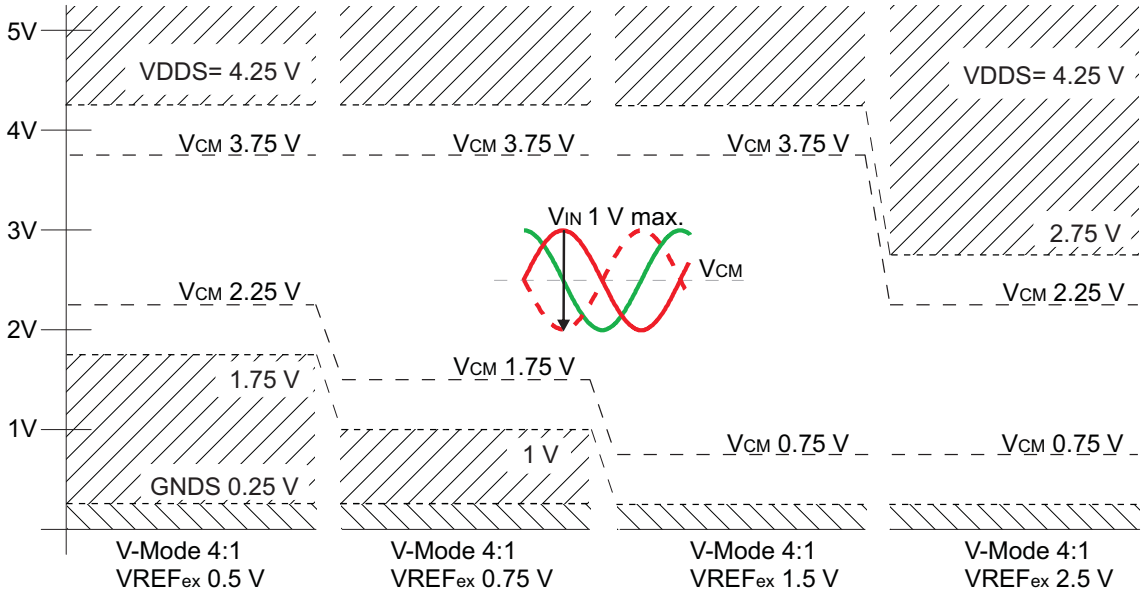


Figure 13: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G12_{eff}$ = 2.0 and V-Mode 4:1.



Notes: MUX(5:4) = 3, $GR12_{eff}$ = 2; $VREF_{ex}$ and $VREF_{in}$ are referenced to GNDS.

Figure 14: Permissible maximum input amplitude V_{IN} and common mode input range V_{CM} for $G12_{eff}$ = 2.0 and V-Mode 4:1 in dependancy to the reference voltage.

Signal Path Multiplexer

The input signals for the index channel CH0 are always taken from the inputs X1 and X2.

The input signals for the channels CH1 and CH2 are taken from the inputs X3 to X6 according to the multiplexer settings in Table 21.
In any case input X4 is linked to PCH1i, the positive signal input of channel CH1.

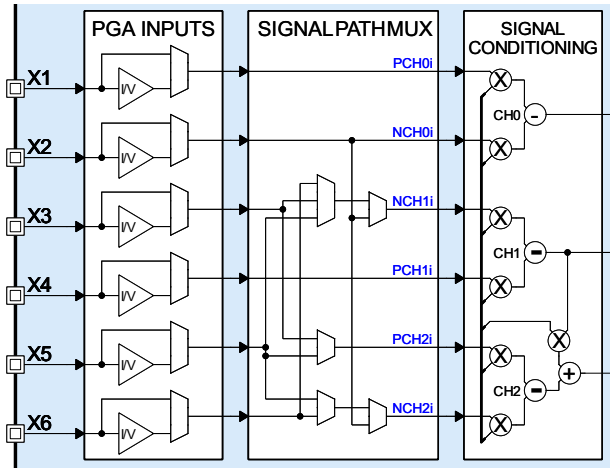


Figure 15: Signal Path Multiplexer

MUX(6:0)	Addr. 0x03, bit 6:0						
Code	Function	PCH2i	NCH2i	PCH1i	NCH1i	PCH0i	NCH0i
any	Fixed assignment (default)			X4		X1	X2
MUX(2:0)	Addr. 0x03, bit 2:0						
0	**Differential input** configuration	X3	X5		X6		
2	Single crossing	X3	X6		X5		
3	Double crossing	X5	X6		X3		
4	**Single-ended** input configuration	X3	X2		X2		
7	Single crossing	X5	X2		X2		
MUX(3)	Addr. 0x03, bit 3						
0	Default assignment					→ PCH0o	→ NCH0o
1	Index signal inversion					→ NCH0o	→ PCH0o
MUX(5:4)	Addr. 0x03, bit 5:4						
0	Default assignment $VREF_{in12} = VREFI_{12}$ $VREF_{in0} = VREFI_0$						X2
2	X2 Output function $VREF_{in12} = VREF_{in0} = VREFI_{12}$ $VREFI_{12}$ is output to X2						VREFI → X2
3	X2 Reference input function $VREF_{in12} = VREF_{in0} = VREF_{ex}$ External $VREF_{ex}$ is input to X2						X2 ← $VREF_{ex}$
MUX(6:0)	Addr. 0x03, bit 6:0						
Code	Function	Pin PB	Pin NB	Pin PA	Pin NA	Pin PZ	Pin NZ
	Default assignment	PCH2o	NCH2o	PCH1o	NCH1o		
0x40	TEST 6 (MODE = 0x6) OpAmp bypass function	X3	X5	X4	X6	X1	X2
Notes	MUX(6:0): Settings which are not explicitly specified may lead to an undesired chip function. MUX(2): The function is compatible to the function of INMODE described for iC-MSB and iC-MQ. MUX(3): The function is compatible to the function of INVZ described for iC-MSB and iC-MQ. MUX(5:4): The function is compatible to the function of BIASEX described for iC-MSB and iC-MQ.						

Table 21: Input Multiplexer Function, Input Signal Mode, and Reference Selection

SIGNAL CONDITIONING CH1, CH2

It is recommended to use operating mode *Test 5* for the calibration of the sine signals. The sine signals are also available in operating mode *Calibration 2* for reasons of compatibility with iC-MQ, but the amplitudes are smaller (just 250 mVpeak instead of 1.5 Vpeak using mode *Test 5*).

Alternatively, characteristic digital test signals are available for offset, amplitude and phase conditioning in operating mode *System Test*.

Gain Settings

The gain is set in four steps:

1. The signal level control is to be shut down and the constant current source for the ACO output is set to a suitable output current (register ACOT = 0x2, ACOR and ACOS values close to the later operating point).

2. The coarse gain factor GR12 is to be selected so that differential signal amplitudes of approx. 6 Vpp are to be produced in operating mode *Test 5* (signal PSIN versus NSIN and PCOS versus NCOS).

3. Using fine gain factor GF2, the cosine signal amplitude is then to be adjusted to be exactly 6 Vpp.

4. The sine signal amplitude can then be adjusted to the cosine signal amplitude via fine gain factor GF1.

This results in a total gain of GR12 x GFi for differential input signals.

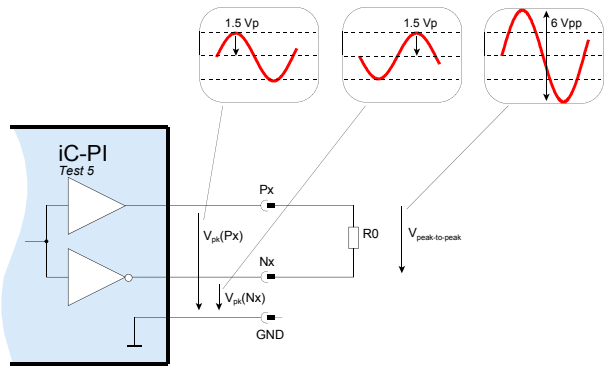


Figure 16: Definition of 6 Vpp differential test signal. Termination R0 must be high-impedance (resistive) during all *Test* and *Calibration* modes.

GR12	Addr. 0x0a, bit 2:0	
Code	Factor with input voltage divider (R12 = 0x9)	Factor w/o input voltage divider (R12 ≠ 0x9)
0x0	3.0	12.0
0x1	6.0	24.6
0x2	7.8	31.8
0x3	10.2	40.2
0x4	13.2	52.2
0x5	15.6	63.0
0x6	19.8	79.2
0x7	24.0	96.0
Notes	The values listed apply for all operating modes except for *Calibration 2* (reduces gain to 1/6). The effective total gain is calculated using: $G12_{eff}$ = GFx x GR12, or $G12_{eff}$ = 1/4 x GFx x GR12 if using the input voltage divider (R12 = 0x9).	

Table 22: Coarse Gain Factor CH1, CH2

GF2	Addr. 0x0c, bit 4:0
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF2}{31}}$
0x1F	6.25

Table 23: Fine Gain Factor CH2

GF1	Addr. 0x0b, bit 6:0, Addr. 0x0a, bit 7:4
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25^{\frac{GF1}{1984}}$
0x7FF	6.6245

Table 24: Fine Gain Factor CH1

Offset Calibration CH1, CH2
In order to calibrate the offset, the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders, iC-PI tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end, the center potentials for the VDC offset references can be adjusted to minimize their AC ripple, using parameters MP1 for VDC1, and MP2 for VDC2 (refer to the k factor of Table 26).

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled sensor current source or by supply VDDS.

VOS12	Addr. 0x05, bit 5:4
Code	Type of source
0x0	Feedback of ACO pin voltage: V(ACO)/20 for supply-dependent differential voltage signals for Wheatstone sensor bridges to measure VDDS
0x1, 0x2	Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensor or waveform generator)
0x3	Self-tracking sources VDC1, VDC2 (125...250 mV) for differential current signals for differential voltage signals*
Notes	*) Requires MUX(5:4) = 3 and the sensor's reference connected to input X2; refer to Elec. Char. No. 111 for acceptable input voltage).

Table 25: Offset Reference Source CH1, CH2

MP1 **MP2**	Addr. 0x0E, bit 1:0; Addr. 0x0D, bit 7:0 Addr. 0x0F, bit 5:0; Addr. 0x0E, bit 7:4
Code	$VDCi = (1 - k) \cdot VPi + k \cdot VNi$
0x000	$k = 1/3$
0x001	$k = 0.3337$
...	$k = 1/3 + 1/3 \cdot Code/1023$
0x200	$k = 0.5000$ (center setting)
...	...
0x3FF	$k = 2/3$
Notes	Adjustment is required only if VOS12 = 0x3

Table 26: VDC Center Potential CH1, CH2

The offset calibration range for CH1 and CH2 is set using the coarse offset factors OR1 and OR2. Both sine and cosine signals are then calibrated using the fine offset factors OF1 and OF2. The calibration target is reached when the DC component of the differential signals PCHi to NCHi is zero.

OR1 **OR2**	Addr. 0x10, bit 1:0 Addr. 0x10, bit 3:2
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 27: Coarse Offset Factor CH1, CH2

OF1 **OF2**	Addr. 0x11, bit 6:0; Addr. 0x10, bit 7:4 Addr. 0x13, bit 2:0; Addr. 0x12, bit 7:0
Code	Factor
0x000	0
0x001	0.00098
...	$+ Code/1023$
0x3FF	+ 1
0x400	0
0x401	− 0.00098
...	$-(Code - 1024)/1023$
0x7FF	− 1

Table 28: Fine Offset Factor CH1, CH2

Phase Correction CH1 to CH2
The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration, other calibration parameters may have to be readjusted (those as amplitude compensation, VDC center potentials and offset voltages).

PH12	Addr. 0x14, bit 5:0; Addr. 0x13, bit 7:4
Code	Correction angle
0x000	0 °
0x001	+ 0.0204 °
...	$+ 10.42° \cdot Code/511$
0x1FF	+ 10.42 °
0x200	0 °
0x201	− 0.0204 °
...	$-10.42° \cdot (Code - 512)/511$
0x3FF	− 10.42 °

Table 29: Phase Correction CH1 to CH2

SIGNAL CONDITIONING CH0

Input Mode CH0

DUAL configures the channel CH0 to process either analog or digital input signals.

DUAL	Addr. 0x07, bit 7
Code	Mode
0x0	Analog input function
0x1	2-bit digital input function

Table 30: Dual Input Mode

When the inputs are configured to analog (DUAL = 0), the gain and offset signal conditioning parameters described further below are operational.

When configured for digital signals (DUAL = 1), the inputs X1 (for PCH0) and X2 (for NCH0) evaluate a 2-bit Gray-coded multiturn signal. Using this code, the repeated signal cycles generated by a magnetoresistive angle sensor or an optical polarization sensor can be distinguished.
To do so, iC-PI interprets the upper bit on X1 (PCH0) as period information, and uses the lower bit on X2 (NCH0) to synchronize the multiturn information to the internal angle position derived form the sine/cosine signals of CH1 and CH2.

Gain Settings CH0

For analog input mode (DUAL = 0), the test signals required to calibrate the zero channel are available in mode *Calibration 1*.
Additionally, the relative phase of the ungated zero signal Z_{In} compared to A and B can be determined in mode *System Test*.

The CH0 gain is set using the following steps:

1. The signal level control is to be shut down and the constant current source for the ACO output is set to the same values as during the calibration of CH1 and CH2 (registers ACOT, ACOR and ACOS).

2. The coarse gain is to be selected so that a differential signal amplitude of approx. 1 Vpp is produced internally (signal PCH0 to NCH0).

3. GF0 then permits fine gain adjustment to 1 Vpp. The total gain is GR0 x GF0.

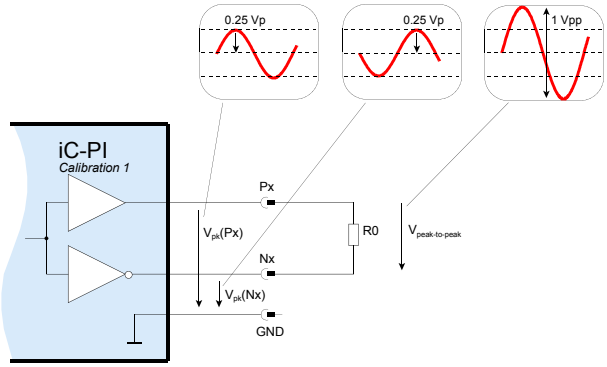


Figure 17: Definition of 1 Vpp differential test signal. Note that the outputs should not be loaded during *Test* and *Calibration* modes (R0 must be high resistance).

Note: Using mode *Test 5* is not recommended, as the CH0 outputs are not buffered.

GR0	Addr. 0x07, bit 6:4	
Code	Factor with input voltage divider (R0 = 0x9)	Factor w/o input voltage divider (R0 ≠ 0x9)
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0
Notes	The effective total gain is calculated using: $G0_{eff}$ = GF0 x GR0, or $G0_{eff}$ = 1/4 x GF0 x GR0 if using the input voltage divider (R0 = 0x9).	

Table 31: Coarse Gain Factor CH0

GF0	Addr. 0x08, bit 4:0
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF0}{31}}$
0x1F	6.25

Table 32: Fine Gain Factor CH0

Offset Calibration CH0

The offset reference source is selected with VOS0. The offset compensation is set with OR0 and OF0 (see Offset Calibration CH1 and CH2 for further information).

VOS0	Addr. 0x04, bit 5:4		
Code	Source	Code	Source
0x0	0.05 · V(ACO)	0x2	0.25 V
0x1	0.5 V	0x3	VDC1

Table 33: Offset Reference Source CH0

OR0	Addr. 0x07, bit 1:0		
Code	Range	Code	Range
0x0	x1	0x2	x6
0x1	x2	0x3	x12

Table 34: Coarse Offset Factor CH0

OF0	Addr. 0x09, bit 5:0
Code	Factor
0x00	0
0x01	0.0322
...	+ *Code*/31
0x1F	1
0x20	0
0x21	− 0.0322
...	− (*Code* − 32)/31
0x3F	− 1

Table 35: Fine Offset Factor CH0

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

iC-PI's signal level controller can keep the input signals for the sine-to-digital converter constant, regardless of temperature and aging effects, when using control output ACO to track the sensor supply.

ACOR(1:0) presets the output current range of pin ACO, the control's highside current source output, and ACOT(1:0) defines its control mode.

The resulting internal signal amplitude and the control's operating range are both monitored and thus can be used for error messaging.

ACOR	Addr. 0x15, bit 7:6
Code	Current range
00	5 mA
01	10 mA
10	25 mA
11	50 mA

Table 36: ACO Output Current Range (applies for control modes and constant current source)

ACOT	Addr. 0x16, bit 1:0
Code	Operating mode
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 37: ACO Output Control Mode

The modes *square control* and *sum control* feature an adjustable deadband, meaning that a deviation of the input signal levels is balanced only if the configured control deadband is exceeded (refer to ACOHYS). Due to this, the control's influence on the sensor's signal quality (regarding THD) can be significantly reduced. The deadband is disabled when configuring a zero hysteresis, so that any deviation of the input levels will be balanced immediately over the ACO output.

ACOHYS	Addr. 0x16, bit 6:4
Code	Hysteresis to setpoint (ACOT = 00)
000	2.5 %
001	5 %
010	7.5 %
011	10 %
1xx	None (continuous control)
Note	This function is available with *square control* and *sum control* modes.

Table 38: Control Deadband

Square Control Mode
The standard control mode is *square control* which uses (sine^2 + cosine^2) to adjust the ACO output current. ACOS(4:0) determines the internal signal amplitudes within the closed-loop control and, simultaneously, the amplitude monitoring thresholds. The ideal setting is when the sin/cos test signals available in operating mode *Test 5* are at 3 Vpp.

ACOS	Addr. 0x15, bit 5:1
Code	**Square control** (ACOT = 00)
0x00	Vpp() ≈ 1800 mV (60 %)
0x01	Vpp() ≈ 1830 mV (61 %)
...	... $\approx 1800\,mV\,\frac{77}{77-(1.25*Code)}$
0x19	Vpp() ≈ 3000 mV (98 %)
...	...
0x1F	Vpp() ≈ 3600 mV (120 %)

Table 39: Square Control Setting (internal sin/cos signal amplitude)

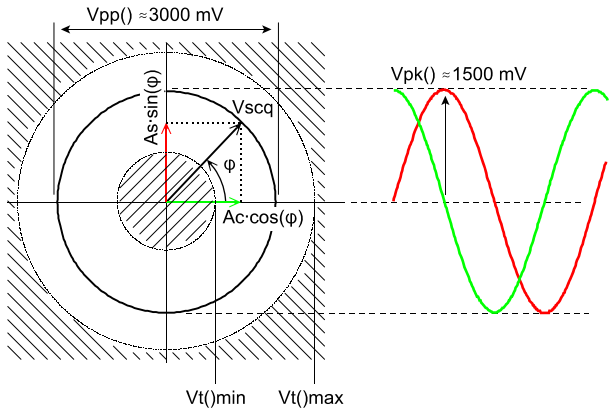


Figure 18: Signal monitoring and test signals in *Test 5* mode (example for ACOS(4:0) = 0x19).

The signal monitoring thresholds are tracked according to ACOS (4:0) and fit for *square control mode*. When using *sum control mode* a different operating point can be required for which the monitoring thresholds may not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

Signal monitoring and thresholds			
ACOS(4:0)	Vt()min ... max	ACOS(4:0)	Vt()min ... max
0x00	0.72 V...2.34 V	0x19	1.2 V ...3.9 V
0x01	0.732 V...2.38 V	...	...
...	...	0x1F	1.44 V...4.68 V
Notes	All values nominal, see also Elec. Char. Nos. 605, 606		

Table 40: Signal Monitoring

Note: Following power up and after the configuration data has been read successfully, the sine/cosine square control starts operation from a zero output current.

Note: Excessive input signals or internal signal clipping can interfere with the control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error 2 and Signal Error 1 for monitoring and configuring EMASKA accordingly.

Sum Control Mode

With *sum control* mode selected, the DC references (VDC1 + VDC2) are used to adjust the output current of pin ACO.

ACOS	Addr. 0x15, bit 5:1
Code	**Sum control** (ACOT = 01)
0x00	VDC1 + VDC2 ≈ 245 mV
0x01	VDC1 + VDC2 ≈ 249 mV
...	... $\approx 245mV\frac{77}{77-(1.25*Code)}$
0x1F	VDC1 + VDC2 ≈ 490 mV

Table 41: Sum Control Setting (DC average)

Constant Current Source

The *constant current source* is intended for signal conditioning purposes, i.e. for the adjustment of gain, offset and phase correction values independent of signal level controlling.

ACOS	Addr. 0x15, bit 5:1
Code	**Constant current source** (ACOT = 10)
0x00	I(ACO) ≈ 3.125% Isc(ACO)
0x01	I(ACO) ≈ 6.25% Isc(ACO)
...	... $\approx 3.125\% * (Code + 1) * Isc(ACO)$
0x1F	I(ACO) ≈ 100% Isc(ACO)
Notes	For tolerances of Isc(ACO) see Elec. Char. No. 602.

Table 42: Current Source Setting (ACO output current)

SINE-TO-DIGITAL CONVERTER

SELRES	Addr. 0x21, bit 6:0; Addr. 0x20, bit 7:0		
Value*	STEP Angle Steps Per Period	IPF Interpolation Factor	fin()max** Permissible Max. Input Frequency
0x0003	4	1	500 kHz
0x0007	8	2	500 kHz
0x000F	16	4	500 kHz
0x0013	20	5	500 kHz
0x001F	32	8	500 kHz
0x0027	40	10	500 kHz
0x003F	64	16	488 kHz
0x004F	80	20	390 kHz
0x0063	100	25	312 kHz
0x007F	128	32	244 kHz
0x009F	160	40	195 kHz
0x00C7	200	50	156 kHz
0x00FF	256	64	122 kHz
0x018F	400	100	78 kHz
0x01F3	500	125	62 kHz
0x01FF	512	128	61 kHz
0x031F	800	200	39 kHz
0x03E7	1000	250	31 kHz
0x03FF	1024	256	30 kHz
0x07CF	2000	500	15 kHz
0x07FF	2048	512	15 kHz
0x0F9F	4000	1000	7.8 kHz
0x0FFF	4096	1024	7.6 kHz
Notes	*) Other settings of SELRES are not allowed. **) According to Elec. Char. 514 for MTD = 0x0; for nominal values refer to Figure 4, page 12.		

Table 43: Converter Resolution

iC-PI's converter resolution is selected with SELRES. For a resolution of 4, four angle steps per input cycle are generated so that the output frequency at A and B matches the sine frequency at the inputs.

The programmable converter hysteresis is determined by SELHYS. It is set in multiples of the increment size and has a maximum of 45° of the input signal period.

SELHYS	Addr. 0x1F, bit 3:0		
Code	Function	Code	Function
0x0	nearly none	0x8	2.0°
0x1	0.09°	0x9	4.0°
0x2	0.18°	0xA	6.0°
0x3	0.36°	0xB	8.0°
0x4	0.54°	0xC	10.0°
0x5	0.72°	0xD	11.25°
0x6	1.0°	0xE	22.5°
0x7	1.5°	0xF	45°

Table 44: Converter Hysteresis

STUPCNT	Addr. 0x21, bit 4
Code	Function
0x0	Suppress edges on ABZ. Duration dependent on the Minimum Edge Distance (MTD). Using the largest MTD, the process lasts up to 15 ms.
0x1	Count from zero angle: burst output to absolute position within input cycle.

Table 45: Converter Startup

HOLDCNT	Addr. 0x21, bit 5
Code	Function
0x0	No Hold on min. amplitude error
0x1	Hold on min. amplitude error

Table 46: Converter Hold on Amplitude Error

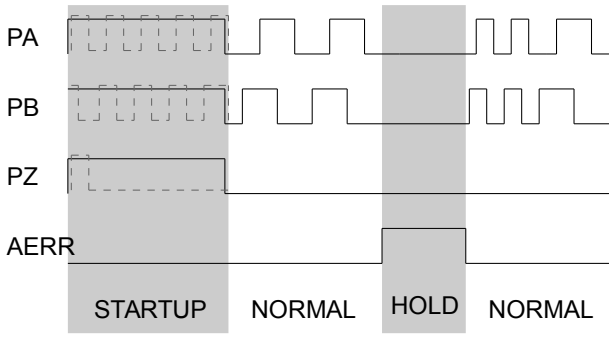


Figure 19: Modes for count signals

Figure 19 shows the device's behavior during the optional startup and hold modes.

STARTUP: When leaving the reset state, the interpolator counts up from zero angle to the applied angle position, at the maximum possible tracking frequency. The bit STUPCNT defines whether the internally counted signals are output at the pins (STUPCNT =1), or supressed (STUPCNT = 0).

NORMAL: After settling, the interpolator tracks the applied input angle in normal mode.

HOLD: In case of a signal error (loss of signal), the sine-to-digital converter is set on hold and no further count pulses can be seen at the outputs (HOLDCNT = 1).

NORMAL: As soon as the amplitude returns back to regular levels, the converter continues counting from the last value and generates as many pulses as required to catch up to the actual position. In doing so, the outputs show the configured minimum edge dis-

tance intermediately. Afterwards, the applied angle is continuously tracked again.

Full-Scale Interpolation (Over 2x 180°)

DUAL	Addr. 0x07, bit 7
Code	Mode
0x0	Analog input function
0x1	2-bit digital input function

Table 47: Dual Input Mode

Utilizing the digital input mode for channel CH0 (DUAL = 1, see Table 47), the signals applied to the inputs X1 and X2 are interpreted as a Gray-coded multiturn position. iC-PI uses this information to distinguish between the first and second half of the mechanical revolution, when sin/cos signals with 2 cycles per turn are applied (refer to input signal X3 in Figure 20).

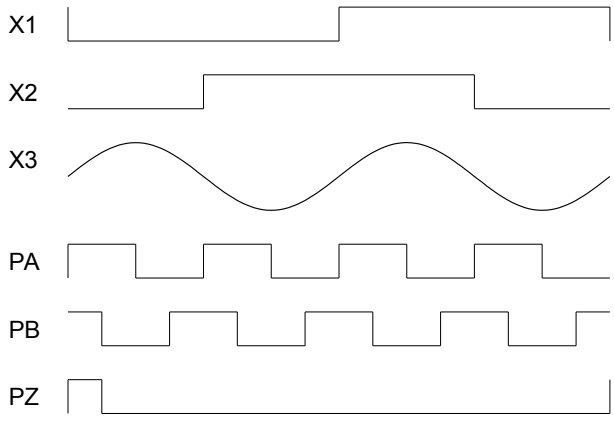


Figure 20: Signal example for interpolation factor x8 (for DUAL = 1).

For X1 and X2, the following pin signals are expected:

Pin X1	Pin X2	Quadrant Information
State	State	Quadrant
0	0	First quadrant
0	1	Second quadrant
1	1	Third quadrant
1	0	Fourth quadrant

Table 48: Quadrant Detection (for DUAL = 1)

The count and index signals change based on the values of three registers: SELRES, CFGZPOS, and DUAL. SELRES determines the conversion resolution and CFGZPOS the angle at which the signal is output. If DUAL = 0 (analog), the signals are output within one sine period, else DUAL = 1 (digital) and the signals are output once per every two sine periods, which correspond to one revolution.

The internal absolute position can be shifted by the register OFFSET. Accordingly, this offset also shifts the incremental signals and the commutation signals. The shift range is within 1 sine period for DUAL = 0, and 2 sine periods for DUAL = 1.

OFFSET	Addr. 0x26, bit 7:0
Code	Absolute position offset
0x00	0°
0x01	1.4°
...	...
0xFF	358.6°

Table 49: Absolute Position Offset

COMMUTATION SIGNALS

Selecting *UVW Mode*, commutation signals become available at pins NA, NB and NZ. The pins PA, PB, and PZ still present the incremental quadrature signals.

The setting of the parameter DUAL is relevant for generating the commutation signals.
For **DUAL = 0**, the commutation signals are derived from the sine input period and are repeated after 1 to 8 fractions of the sine period.
For **DUAL = 1**, the commutation signals are derived from 2 sine input periods and are unique together with the digital word at the input of channel 0. The commutation signals are repeated after 1 to 8 fractions of two sine periods.

POLES	Addr. 0x25, bit 6:4	
Code	Motor Pole Count	UVW Output
0x0	2 poles	1 cpr*, length 360°
0x1	4 poles	2 cpr, length 180°
0x2	6 poles	3 cpr, length 120°
0x3	8 poles	4 cpr, length 90°
0x4	10 poles	5 cpr, length 72°
0x5	12 poles	6 cpr, length 60°
0x6	14 poles	7 cpr, length 51.43°
0x7	16 poles	8 cpr, length 45°
Notes	*) Cycles per revolution with input of 1 sin/cos period per mechanical revolution using DUAL = 0. The setting of POLES is only relevant in *UVW Mode* (MODE = 0x0E).	

Table 50: Pole Count for Commutation Signals

Figure 21 shows the commutation sequence for a motor with 6 pole pairs. Here, a commutation sequence spanning an angle of φ_{360UVW} repeats itself 6 times within one mechanical revolution of the motor's rotor. The phase shift between the commutation signals is 120° related to one signal cycle (360°).

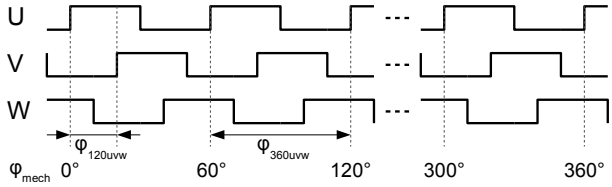


Figure 21: Example of UVW commutation signals.

INDEX GATING

The interpolation factor (IPF) determines the number of A/B signal cycles per input signal period. These A/B signal cycles are counted internally by register POS, to allow an adjustable gating with the external index signal applied to the zero inputs.

POS starts from zero (when the sine/cosine input phase is zero degrees) and reaches POS_{max} = IPF - 1 as its maximum. The internal A/B signal cycle adheres to the following pattern:

A	1	1	0	0
B	1	0	0	1

Table 51: Internal A/B Signal Cycle

Inversions and reversals can be selected for the output of the A/B/Z signals using CFGABZ(7:4), and the zero signal can be gated with any combination of the internal A and B signal using CFGABZ(3:0).

CFGABZ	Addr. 0x1D, bit 7:0
Bit	Function and Description
7	Output inversion for channel A: PA<>NA PA = P1i xor CFGABZ(7)
6	Output inversion for channel B: PB<>NB PB = P2i xor CFGABZ(6)
5	Output inversion for index channel: PZ<>NZ PZ = P0i xor CFGABZ(5)
4	Exchange of the A/B signals 0: P1i = A, P2i = B 1: P1i = B, P2i = A
	Zero Signal Gating CFGABZ(3:0)
3	Enable for A = 1, B = 1
2	Enable for A = 1, B = 0
1	Enable for A = 0, B = 0
0	Enable for A = 0, B = 1

Table 52: Output Logic

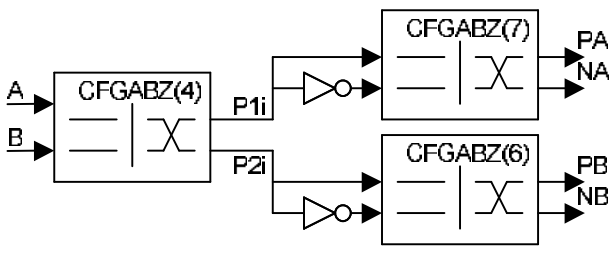


Figure 22: Signal path from A and B to PA/NA and PB/NB

Zero Signal Generation
The zero signal generation depends on the internal window signal Z_{In} which is derived from a comparator evaluating the calibrated index signal input to CH0.

As the width of the window signal Z_{In} varies with the offset calibration of CH0, its correct size and position should be checked ahead of configuring any gating. Using *Mode ABZ*, the internal window signal Z_{In} can be output to pin ERR for inspection (requires EMASKA = 0x010 and EMTD = 0x0).

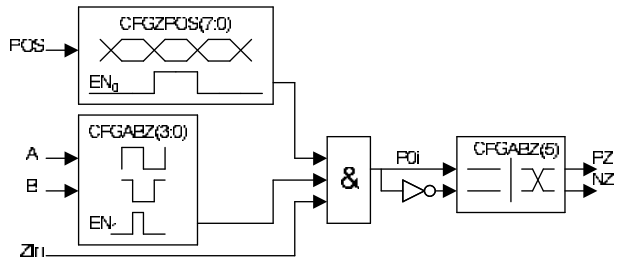


Figure 23: Signal path from Z_{In} to PZ/NZ

The zero signal output to PZ is generated during the A/B cycle where the POS number is equal to CFGZPOS. It is therefore essential that this specific A/B cycle is fully enclosed by the window signal Z_{In}.

CFGZPOS	Addr. 0x1E, bit 7:0
Bit	Description
7	1: Masking enabled 0: Masking disabled
(6:0)	Selection of A/B cycle number: IPF < 200: POS = CFGZPOS(6:0) IPF ≥ 200: POS = 8 * CFGZPOS(6:0)

Table 53: Zero Signal Positioning

Note: The A/B cycle number configured by CFGZPOS must not exceed POS_{max} = IPF - 1.
So when changing the interpolation factor IPF, CFGZPOS must be adapted accordingly.

ENZFF	Addr. 0x02, bit 4
Code	Description
0	Zero signal output with state change of P0i
1	Zero signal output synchronized with A/B signal

Table 54: Zero Signal Synchronization

Zero Signal Output Logic

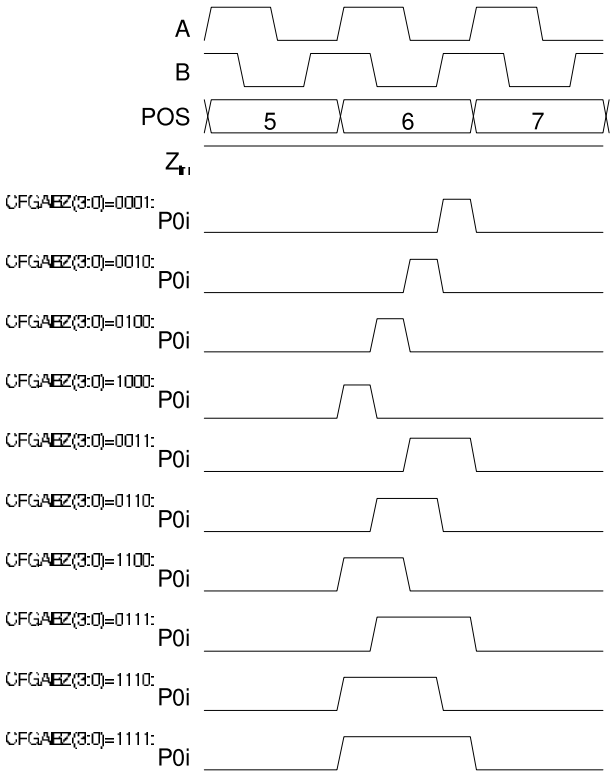


Figure 24: Zero signal gating by CFGABZ(3:0); Example for CFGZPOS(7) = 1, and CFGZPOS(6:0) = 0x6.

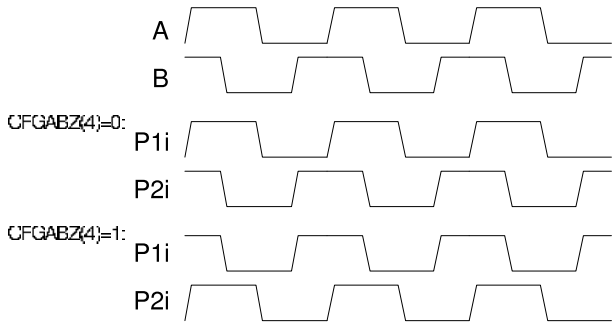


Figure 25: Function of CFGABZ(4)

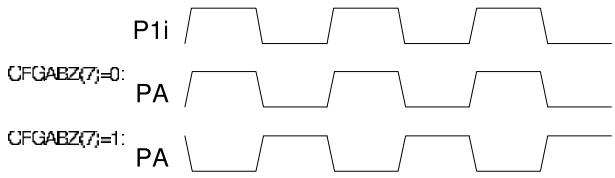


Figure 26: Function of CFGABZ(7)

Configuration Example 1
Incremental ABZ output with a zero signal of 180° synchronous with the A signal at PA:
CFGABZ = "0000 1100"

Configuration Example 2
Incremental ABZ output with a zero signal of 270° which can be synchronized externally with a 90° zero pulse for PA = 1 und PB = 1:
CFGABZ = "1100 0111"

OUTPUT DRIVERS

The output drivers can be used as push-pull, lowside or highside drivers, or can be switched off (tristate); the mode of operation is determined by TRIHL(1:0).

The slew rate can be set using SSR to suit the length of the cable. Lower slew rates are used to avoid steep edges when transmitting via short wires, but can result in a limiting of the maximum permissible output frequency. For example, this frequency is 300 kHz at a slew rate of 300 ns if the RS422 specification is to be adhered to. The tolerances in Electrical Characteristics, numbers 505 and 506, must be observed.

The short-circuit current can be set by SIK and can be minimized when connecting to on board logic or to an external 24 V line driver. If the outputs are used as RS422-compatible 5 V drivers, it is recommended that SIK = 11 to keep the power dissipation of iC-PI low.

TRIHL	Addr. 0x22, bit 1:0
Code	Function
00	Push-pull operation
01	Highside driver mode (P channel open drain)
10	Lowside driver mode (N channel open drain)
11	Tristate

Table 55: Output Drive Mode

SSR	Addr. 0x22, bit 3:2
Code	Function
00	Nominal value 12 ns
01	Nominal value 25 ns
10	Nominal value 80 ns
11	Nominal value 220 ns
Note	For tolerances see Elec. Char. Nos. 505 and 506.

Table 56: Output Slew Rate

SIK	Addr. 0x22, bit 5:4
Code	Function
00	typ. 2 mA, linking logic or driver ICs
01	typ. 8 mA
10	typ. 40 mA
11	typ. 100 mA, recommended for RS422
Note	For tolerances see Elec. Char. Nos. 503 and 504.

Table 57: Output Short-Circuit Current

Minimum Edge Distance and Noise Filter

MTD	Addr. 0x1F, bit 7:4	
Code	t_{MTD} during *ABZ Mode*, and *UVW Mode*	tclk()lo during *191/193 Mode*
0x0	25 ns	not available
0x1	50 ns	25 ns
0x2	75 ns	25 ns
0x3	100 ns	50 ns
0x4	125 ns	50 ns
0x5	150 ns	75 ns
0x6	200 ns	100 ns
0x7	300 ns	150 ns
0x8	400 ns	200 ns
0x9	550 ns	275 ns
0xA	800 ns	400 ns
0xB	1.0 µs	500 ns
0xC	1.3 µs	650 ns
0xD	1.6 µs	800 ns
0xE	3.2 µs	1.6 µs
0xF	6.4 µs	3.2 µs
Note	All timing specifications are nominal values. Refer to Elec. Char. 514 and 515 for tolerances.	

Table 58: Minimum Edge Distance

The minimum edge distance of the output signals can be preset by MTD(3:0). This setting limits the maximum possible output frequency to ensure a safe transmission to counters, which permits only a low input frequency and thus cannot resolve glitches. The configuration of the RS422 output drivers (with regard to the driver current and slew rate) and the cable length must be taken into account when choosing the minimum edge distance.

ENF	Addr. 0x03, bit 7
Code	Function
0	Disabled
1	Noise limiting signal filter enabled (default)

Table 59: Noise Filter

MONITORING AND ERROR OUTPUT

iC-PI monitors the input signals, the internal interpolator and the sensor supply controller through which the input signal levels are stabilized. If the sensor supply tracking unit reaches its control limits this can be interpreted as an end-of-life message, for example.

Three separate error masks stipulate whether error events are signaled as an alarm via I/O pin ERR (mask EMASKA), whether they cause the (RS422) output drivers to shutdown or not (mask EMASKO) or whether they are stored in the EEPROM (mask EMASKE).

Error Input/Output: pin ERR

Pin ERR is operated by a current-limited open-drain output driver and has an internal pull-up which can be disabled. The ERR pin also acts as an input for external system error messaging. Interpretation of an external system error message and the phase of the message output is configured by EPH and the minimum indication time by EMTD.

EPH	Addr. 0x1A, bit 4	
Code	State on internal error	State w/o internal error
0*	active low	high impedance; input function for external system error is low-active;
1	high impedance	active low
Notes	*) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case.	

Table 60: I/O Logic, Alarm Output ERR

EMTD	Addr. 0x18, bit 6:4		
Code	Indication Time	Code	Indication Time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 61: Min. Indication Time, Alarm Output ERR

EPU	Addr. 0x1A, bit 5
Code	Function
0	No internal pull-up
1	Internal 300 µA pull-up current source active

Table 62: Pull-Up Enable, Alarm Output ERR

EMASKA	Addr. 0x18, bit 1:0; Addr. 0x17, bit 7:0
Bit	Error event
9	Line count error: wrong count of sine periods between two zero pulses
8	Excessive output lag: output angle differs from actual input angle, e.g. after cycling power, when exceeding the maximum input frequency, when the output frequency is limited due to the minimum edge distance (MTD)
7	Excessive input frequency: angle lost by interpolation engine (at ≈ 600 kHz***)
6*	Configuration error: checksum error, no acknowledge signal from EEPROM, or SDA or SCL pin error.
5	Excessive temperature warning
4	Ungated index enable signal Z_{In} (comparated X1/X2 inputs for CFGABZ and CFGZPOS adjustment, at EMTD = 0x0)
3	Control range at max. limit (control error 2)
2	Control range at min. limit (control error 1)
1	Signal clipping (signal error 2)
0	Loss of signal (signal error 1): poor differential amplitude**, wrong s/c phase.
Code	Function
1	Enable: event changes state of pin ERR (if EMASKO does not disable the output function).
0	Disable: event does not affect pin ERR.
Notes	*) Pin ERR can not pull low on configuration error, use high-active error logic instead (EPH = 1); **) Also due to excessive input signals or internal signal clipping. ***) Limit does not depend on IPF or MTD, just on the chip's system clock. This error indicates that the digital engine is not able to capture the input signals anymore.

Table 63: Error Mask Alarm Output ERR

Line Count Error

Line count monitoring is of particular importance for encoder systems. iC-PI counts the number of sine cycles between two adjacent zero pulses and compares it to the reference value LINECNT. In case of a deviation, the line count error is set. The check is paused if the direction of rotation changes, and is restarted on the next zero pulse.

LINECNT	Addr. 0x24, bit 5:0; Addr. 0x23, bit 7:0	
Code	Function Value	Line Count (CPR)
0x0000	0	1
...	...	*Code* + 1
0x3FFF	16383	16384
Example	Code disc of 256 CPR → LINECNT = 255	

Table 64: Line Count Reference

Excessive Temperature Warning

Exceeding the temperature warning threshold T_w (corresponds to T_2, refer to Temperature Sensor, page 21) can be signaled at pin ERR or used to shut down the output drivers (via mask EMASKO). The temperature warning is cleared if the temperature falls below $T_w - T_{hys}$.

Note: If the temperature shutdown threshold $T_{off} = T_w + \Delta T$ is exceeded, the output drivers are shut down independently of EMASKO. For ΔT refer to Elec. Char. E07.

Configuration Error

The chip's internal configuration registers (RAM addresses 0x00 to 0x2E) are permanently reviewed and verified by the checksum CHKSUM stored at address 0x2F. If the CRC verification fails, the configuration error will be asserted (as also when the initial configuration from the EEPROM fails).

Output Driver Shutdown

Output driver shutdown is a precaution to protect iC-PI. During shutdown, the output drivers and pin ERR are tristate, and the output current range for pin ACO is reset to the 5 mA range.

Driver shutdown due to overheating or due to a configuration error is always enabled. Configuration errors are SDA or SCL pin error, no acknowledge signal from EEPROM or invalid checksum. EMASKO is used to configure driver shutdown due to other error events.

PDMODE	Addr. 0x1A, bit 6
Code	Function
0	Driver shutdown terminates with the error event
1	Permanent driver shutdown until cycling power

Table 65: Driver Activation

EMASKO	Addr. 0x1A, bit 1:0; Addr. 0x19, bit 7:0
Bit	Error event
9:5, 3:0	Refer to the description of EMASKA.
4	External system error: I/O pin ERR pulled to low by an external error signal (using EPH = 0)
Code	Function
1	Enable: event causes a driver shutdown
0	Disable: output drivers remain active

Table 66: Error Mask Driver Shutdown

Error Logging

Error information can be stored in the EEPROM. Only errors enabled by EMASKE are logged. The first error in the lifetime of the product is stored in ERRFIRST. The latest occurred error is stored in ERRACT.

The EEPROM has an additional memory area in which all errors are accumulated (ERRACC). Only errors enabled by EMASKE are logged and only the fact that this error has occurred is logged, with no information as to the time and count of appearance of that error given. Error logging can be used to statistically evaluate the causes of system failure, for example.

iC-PI enters standby and the output drivers are shut down if an I^2C communication error occurs while writing to the EEPROM. iC-PI can be reenabled with bit RUN if EMASKO(6) is zero.

EMASKE	Addr. 0x1C, bit 1:0; Addr. 0x1B, bit 7:0
Bit	Error event
9:5, 3:0	Refer to the description of EMASKA.
4	External system error: I/O pin ERR pulled to low by an external error signal (using EPH = 0)
Code	Function
1	Enable: event will be logged.
0	Disable: event will not be logged.

Table 67: Error Mask EEPROM Savings

Note: The GUI's *Error Display* can only be used, when events of interest are enabled using EMASKE().

ERRFIRST	Addr. 0x31, bit 1:0; Addr. 0x30, bit 7:0
ERRACT	Addr. 0x32, bit 3:0; Addr. 0x31, bit 7:2
ERRACC	Addr. 0x33, bit 5:0; Addr. 0x32, bit 7:4
Bit	Error Event
9:0	Assignation according to EMASKA
Code	Function
0	No event
1	Logged error event

Table 68: Error Protocol

Clearing Errors

Using an external I^2C master device connected to the I^2C bus, the error information in the RAM and in the EEPROM (ERRFIRST, ERRACT, and ERRACC on addresses 0x31 to 0x33) can be cleared at any time. However, if an error condition is active in the iC-PI which is enabled to be logged, iC-PI will update the error memory as soon as the I^2C bus is available again.

Note: Any write access to change a parameter will trigger a configuration error, which persists until the checksum CHKSUM was adapted. When using error logging, also the error memory needs to be cleared finally.

Note: Setting RUN = 0 does not stop iC-PI's error management completely, but stops the incremental engine and thus the generation of a line count error, a tracking error and an excessive input frequency error (registers ERRxxx(9:7)).

REVERSE POLARITY PROTECTION

iC-PI is protected against a reversal of the supply voltage and has short-circuit-proof, error-tolerant output drivers. A defective device cable or one wrongly connected is tolerated by iC-PI. All circuitry components which draw the monitored supply voltage from VDDS and GNDS are also protected.

The following pins are also reverse polarity protected: PA, NA, PB, NB, PZ, NZ, ERR, VDD, GND and ACO.

Conditions: This is based on the condition that GNDS only receives load currents from VDDS. The maximum voltage difference between GNDS and another pin should not exceed 6 V (respectively 8 V for pin ERR).

Note: If iC-PI detects reverse polarity on power up, the line drivers will not be enabled.
If the state of reverse polarity is resolved, iC-PI reboots from the EEPROM and enables the line drivers.

APPLICATION NOTES: SIGNAL CONDITIONING

The precise setting of the signal conditioning unit for correction of the analog input signals is essential to the result of interpolation; the absolute angle error obtained determines the minimum signal jitter. Here, the effect on the transition distance of the A/B output signals is not always the same but instead dependent on the absolute phase angle of the input signals. The following gives an example for an interpolation factor of 100, i.e. 400 edges per sine period.

The offset error in the cosine signal has the strongest effect on the absolute angle error at 90° and 270°; at 0° and 180° its influence on the transition distance is the most marked. With a range setting of OR1 = OR2 = 00 and VOS12 = 01 (selects V05 of 500 mV) the offset error can be compensated in increments of 0.5 mV. If the offset has been compensated for incorrectly by one step (1 LSB), the absolute angle error would increase by approx. 0.06° and the transition distance vary by approximately ± 0.1 %. Similar conditions apply to the sine signal, with the sole difference that the maxima would be shifted by 90°.

An error in amplitude has the strongest effect on the absolute angle error at 45°, 135°, 225° and 315°; the biggest change in the transition distance can be observed at 0°, 90°, 180° and 270°. iC-PI can compensate for the amplitude ratio in steps of approx. 0.1 % so that incorrect compensation by 1 LSB would increase the absolute angle error by approx. 0.06°. The transition distance would then vary by ± 0.1 %.

A phase error between the sine and cosine signals (a deviation in phase shift from the ideal 90°) has the most marked influence on the absolute angle error at 0°, 90°, 180° and 270°. The greatest effect on the transition distance is noted at 45°, 135°, 225° and 315°. iC-PI's phase correction feature permits a step size of 0.02° so that incorrect compensation by 1 LSB would increase the absolute angle error by approx. 0.02°. The transition distance would then vary by ± 0.03 %.

In a perfect signal conditioning procedure it can be assumed that the residual error constitutes half a compensation step. With this, in theory iC-PI would achieve an absolute angle accuracy of approx. 0.03°, with the transition distance varying by approx. ± 0.05 %. Additionally, the linearity error of the interpolator must also be taken into consideration; this increases the absolute angle error by approx. 0.13° and the variation in transition distance by approx. 0.5 % (refer to the Electrical Characteristics No. 302, and 304 for further ratings).

MODE(3:0)		Addr. 0x02; bit 3:0						
Code	Operating Mode	Pin PA	Pin NA	Pin PB	Pin NB	Pin PZ	Pin NZ	Pin ERR
0x00	ABZ	A+	A-	B+	B-	Z+	Z-	ERR
0x0E	UVW	A+	U	B+	V	Z+	W	ERR
0x01	Calibration 1	res.	res.	res.	IBN*	PCH0	NCH0	res.
0x02	Calibration 2	**PCH1**	**NCH1**	**PCH2**	**NCH2**	**VDC1**	**VDC2**	res.
0x0B	System Test**	$\mathbf{A}_8$	$\mathbf{A}_4$	$\mathbf{B}_8$	$\mathbf{B}_4$	Z_{In}	TP1	ERR
		*) Outputs must be active and not tristate (see note on page 21). **) Additional parameter settings are required, see page 23, Table 18. Note that the input frequency may not exceed 1 kHz.						

Table 69: Selected operating modes and test signals.

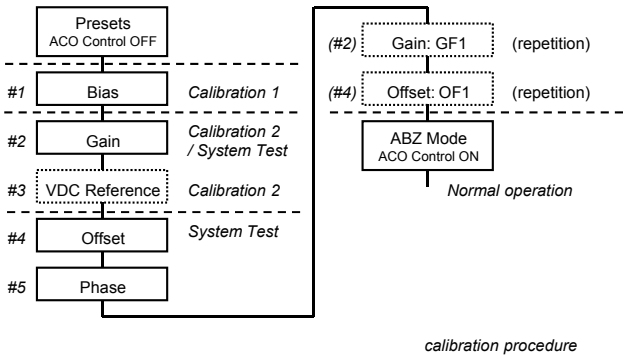


Figure 27: Principle approach
(shown for channel CH1 and CH2).

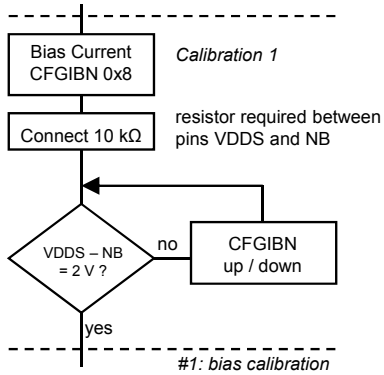


Figure 28: Verification of the bias current is recommended, and if necessary adjustment (see chapter bias current source).

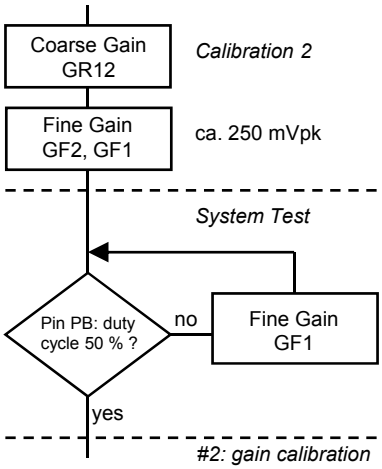


Figure 29: Adjustment of coarse gain GR12 and fine gains GF1 and GF2 to obtain the target amplitude of 250 mVpeak. Amplitude matching is adjusted by fine gain control GF1 of channel CH1.

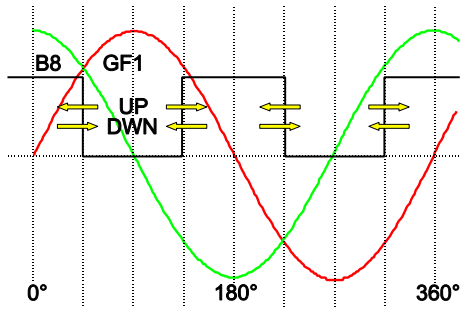


Figure 30: Test signal at pin PB for fine tuning of channel CH1 for identical amplitudes. The adjustment is ideal at a duty ratio of 50%.

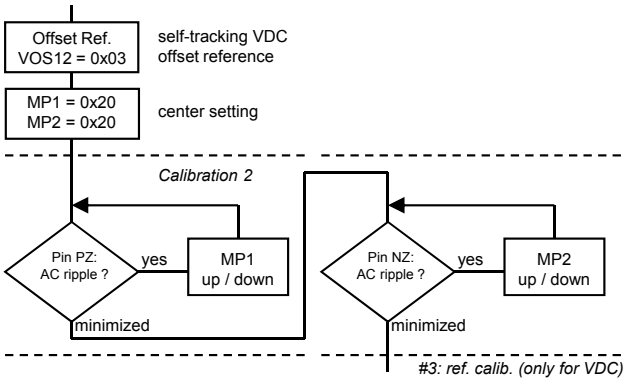


Figure 31: When using the self-tracking VDC offset references, an adjustment of the VDC center potentials for minimal AC ripple is advisable. Other offset references do not require this adjustment.

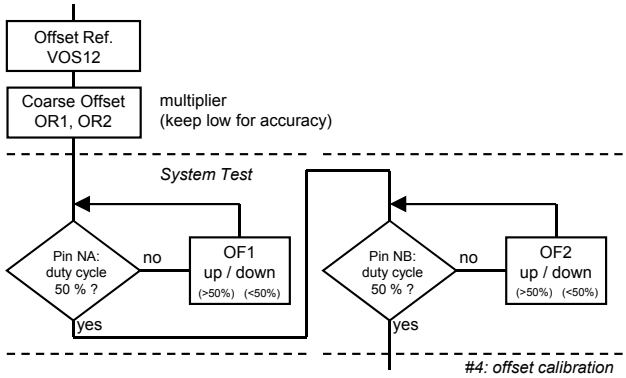


Figure 32: Selection of coarse offset OR1 and OR2 and the subsequent calibration of OF1 and OF2. Selecting OR1 and OR2 as small as possible permits a finer adjustment.

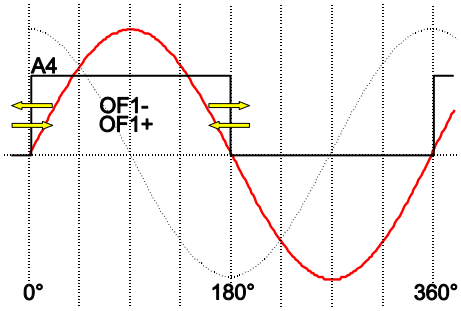


Figure 33: Test signal at pin NA for offset calibration of channel CH1. The adjustment is ideal at a duty ratio of 50%.

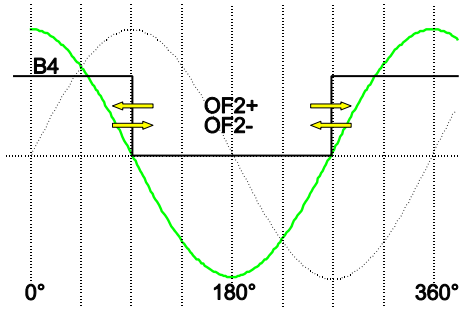


Figure 34: Test signal at pin NB for offset calibration of channel CH2. The adjustment is ideal at a duty ratio of 50%.

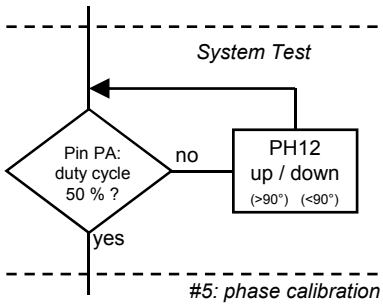


Figure 35: Correction of the sine-to-cosine phase shift by PH12. Repeating the gain and offset calibrations may be reasonable if larger phase correction values are required (refer to chapter signal conditioning for further details).

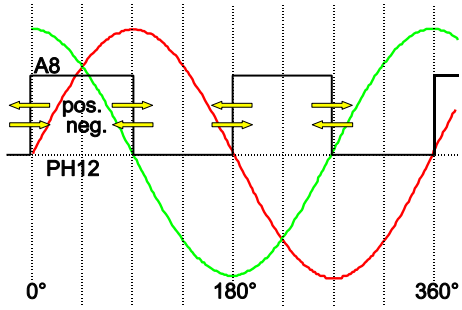


Figure 36: Test signal at pin PA for phase calibration of channel CH1 versus CH2. The adjustment is ideal at a duty ratio of 50%.

Offset Quick Check

During normal operation with an interpolation factor of one iC-PI comparates the sine and cosine zero crossing. Connecting a DC voltmeter to the complementary outputs (P versus N output) indicates directly deviations of the duty cycle. Offset-free signals lead to a duty cycle of 50 % and thus to a measurement value of zero Volts ideally.

This measurement method can also be used when line drivers are connected for 24 V applications; just sensitivity is increased.
To obtain stable readings a minimal signal frequency must be selected, what may depend on the voltmeter model.

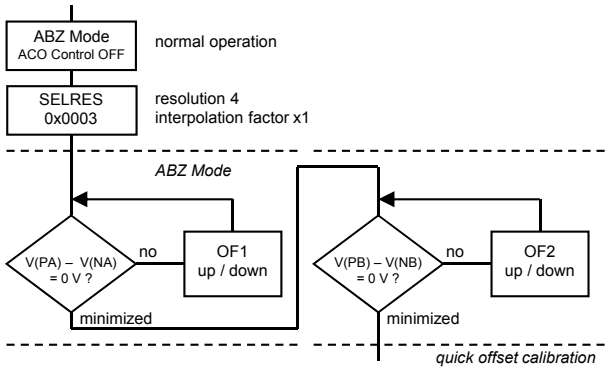


Figure 37: Offset quick check during normal operation with interpolation factor x1.

Signal Conditioning Example 1:
Photodiode array connected to current inputs, LED supply with constant current source

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x3, GF1= 0x400, VDC1= 0x200, OF1= 0x0, GF2= 0x10, VDC2= 0x200, OF2= 0x0 Example: LED current approx. 6.25 mA ACOT(1:0)= 0x2 (constant current source), ACOR(1:0)= 0x3 (range 50 mA), ACOS(4:0)= 0x04 (value 12.5)
2.		Calibration of Channel 1:
	Test 5	Parameter GR12: Adjust the diff. signal at PA to NA to approx. 6 Vpp amplitude
	Test 5	Parameter GF1: Adjust the diff. signal at PA to NA to exactly 6 Vpp amplitude
	Calibration 2	Parameter VDC1: Minimize the AC component of VDC1 at PZ (ripple < 10 mVpeak)
	Test 5	Parameter OR1, OF1: Minimize the DC component of the diff. signal PA to NA (< 5 mVdc)
3.	*Test 5*	Calibration of Channel 2:
	Test 5	Parameter GF2: Adjust the diff. signal at PB to NB to exactly 6 Vpp amplitude
	Calibration 2	Parameter VDC2: Minimize the AC component of VDC2 at NZ (ripple < 10 mVpeak)
	Test 5	Parameter OR2, OF2: Minimize the DC component of the diff. signal PB to NB (< 5 mVdc)
4.	*System Test*	1st Iteration, Calibration of Channel 1 to Channel 2: duty cycle Parameter OF1: Adjust duty ratio of A_4 at NA to 50 % Parameter OF2: Adjust duty ratio of B_4 at NB to 50 % Parameter PH12: Adjust duty ratio of A_8 at PA to 50 % Parameter GF1: Adjust duty ratio of B_8 at PB to 50 %
5.	*Calibration 2*	Repeated Adjustment of VDC Offset References, VDC1 and VDC2: Parameter VDC1: Minimize the AC component of VDC1 at PZ Parameter VDC2: Minimize the AC component of VDC2 at NZ
6.	*System Test*	2nd Iteration, Calibration of Channel 1 to Channel 2: duty cycle Parameter OF1: Adjust duty ratio of A_4 at NA to 50 % Parameter OF2: Adjust duty ratio of B_4 at NB to 50 % Parameter PH12: Adjust duty ratio of A_8 at PA to 50 % Parameter GF1: Adjust duty ratio of B_8 at PB to 50 %

Table 70: Conditioning example 1

Signal Conditioning Example 2:
Encoder supplying 100 mVpp to voltage inputs

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x1, GF1= 0x400, OF1= 0x0, GF2= 0x10, OF2= 0x0
2.		Calibration of Channel 1:
	Test 5	Parameter GR12: Adjust the diff. signal at PA to NA to approx. 6 Vpp amplitude
	Test 5	Parameter GF1: Adjust the diff. signal at PA to NA to exactly 6 Vpp amplitude
	Test 5	Parameter OR1, OF1: Minimize the DC component of the diff. signal PA to NA (< 5 mVdc)
3.	*Test 5*	Calibration of Channel 2:
	Test 5	Parameter GF2: Adjust the diff. signal at PB to NB to exactly 6 Vpp amplitude
	Test 5	Parameter OR2, OF2: Minimize the DC component of the diff. signal PB to NB (< 5 mVdc)
4.	*System Test*	Calibration of Channel 1 vs. Channel 2: duty cycle Parameter OF1: Adjust duty ratio of A_4 at NA to 50 % Parameter OF2: Adjust duty ratio of B_4 at NB to 50 % Parameter PH12: Adjust duty ratio of A_8 at PA to 50 % Parameter GF1: Adjust duty ratio of B_8 at PB to 50 %

Table 71: Conditioning example 2

APPLICATION NOTES: CIRCUIT EXAMPLES

Figure 38 is a circuit diagram of an optical encoder with incremental quadrature outputs as RS422-compatible differential signals which should be terminated by 100 Ω resistors at the controller end. Alternatively, a magnetic encoder using magnetoresistive sensor bridges is shown in Figure 39. Overvoltage protection is realized using TVS diodes and a PolyFuse in the VDD line, as shown.

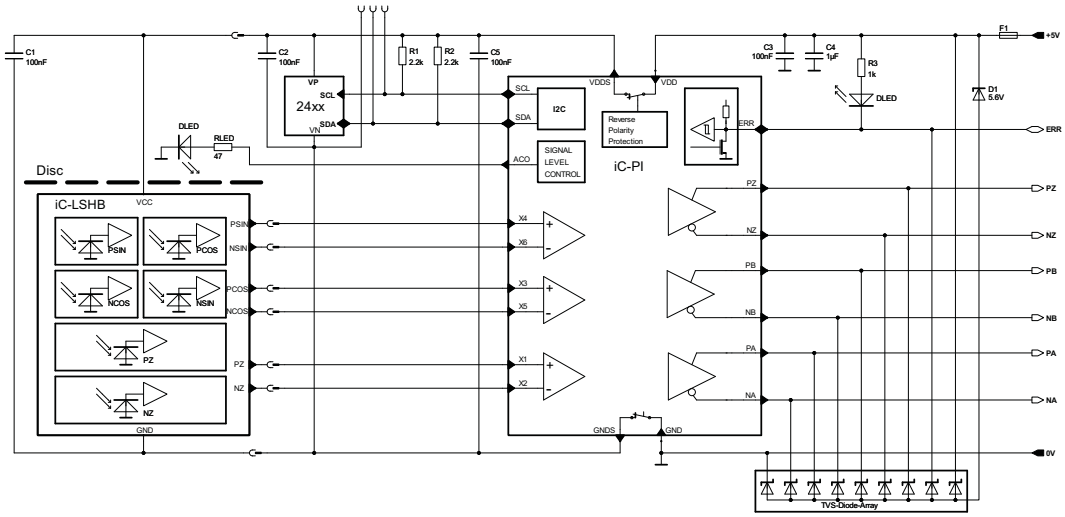


Figure 38: Optical encoder application example.

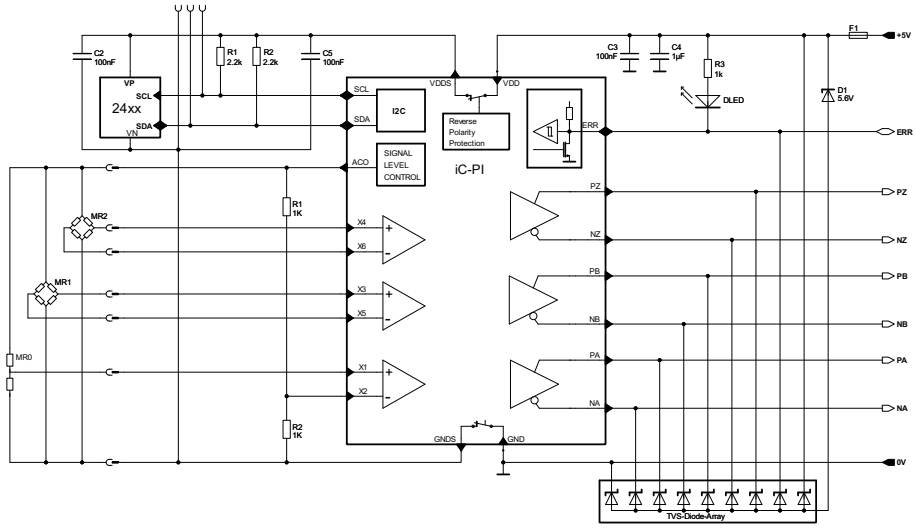


Figure 39: Magnetic encoder application example.

When iC-PI is used in 24 V systems with supply voltages of 5 V to 30 V for example, it can be combined with iC-DL which is a line driver with integrated line adaptation (Figure 40).

Reduced driving capability of iC-PI is sufficient (SIK = 00) to operate iC-DL, so current from the 5 V supply is reduced. If an LDO voltage regulator is selected, the circuit is suitable for a supply range of 4.5 V to 30 V without any change.

The wiring of the iC-DL error message output (pin NER) to the PLC is not necessary if the iC-PI error mask is set for output shutdown (EMASKO). In the event of an error, the pull-down current sources ensure that a low signal is produced at the iC-DL inputs on all lines. The

controller recognizes this condition as an error. If there is an overload at the outputs, the iC-DL itself—via its temperature protection feature—makes sure that the driver outputs are shut down (tristate). The controller also recognizes this as an error. In addition, iC-PI can record the overload condition in its error memory as a system error when using the bidirectional I/O pin ERR (as shown).

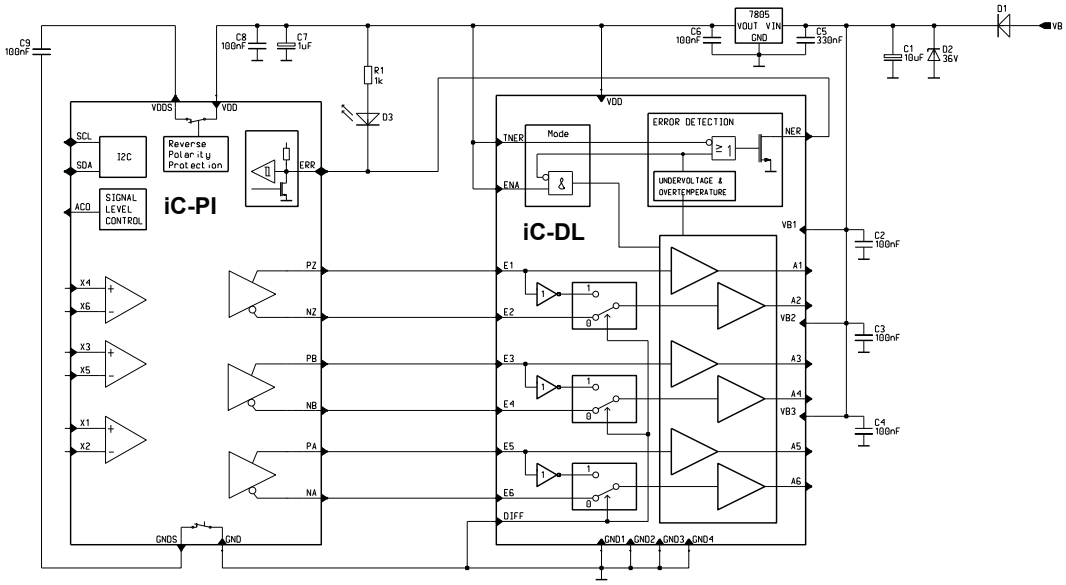


Figure 40: Application example with 24 V line driver.

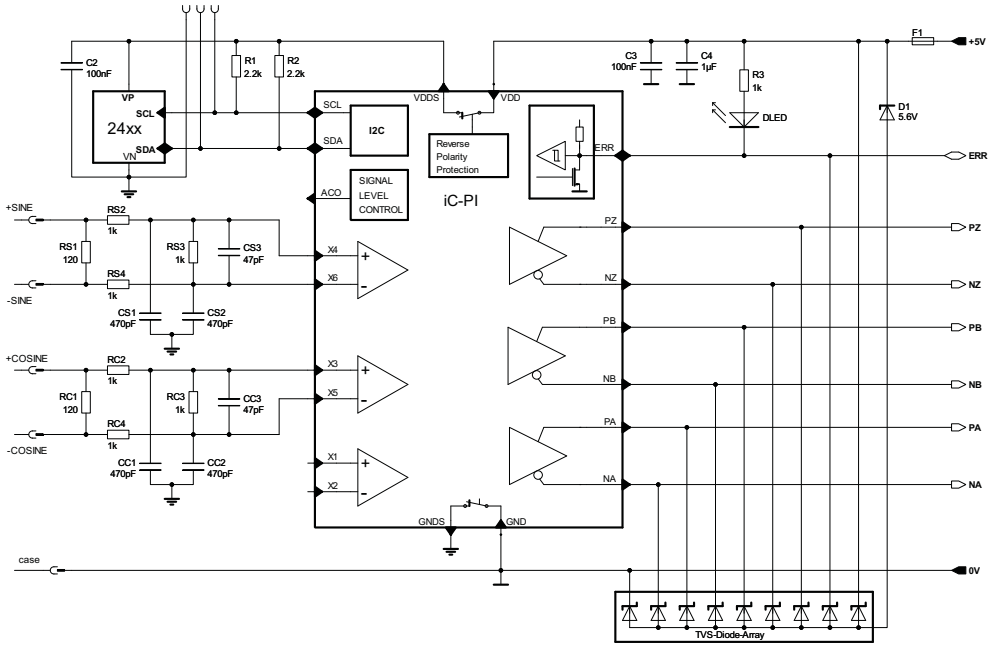


Figure 41: Input circuit for sine encoders (0.8 Vpp to 1.2 Vpp) with 120 Ω termination and low-pass filtering. RS2/RS4 and RC2/RC4 serve as protection against ESD and transients. RS3 and RC3 reduce the input signal levels to 1/3 suiting for an overall gain of 18 (GR12 x GF1, resp. G12 x GF2).

DESIGN REVIEW: Function Notes

iC-PI Y, Y1		
No.	Function, Parameter/Code	Description and Application Notes
		For former chip releases, refer to datasheet release A1.

Table 72: Notes on chip functions regarding iC-PI chip release Y, Y1.

iC-PI X		
No.	Function, Parameter/Code	Description and Application Notes
1	I^2C Slave Function	Using a block-wise I^2C access is possible for reading data from the chip's RAM, but not for writing data to the RAM.

Table 73: Notes on chip functions regarding iC-PI chip release X.

REVISION HISTORY

Rel.	Rel. Date†	Chapter	Modification	Page
A1	2017-11-10		Initial release	

Rel.	Rel. Date†	Chapter	Modification	Page
B1-3	2018, 2019		Refer to the revision history of the release.	

Rel.	Rel. Date†	Chapter	Modification	Page
B4	2019-05-20	SERIAL I^2C INTERFACE	Figure 5 and Table 4 added, description updated; EEPROM Device Requirements: Table 5: correction of max. EEPROM size to 8 Kbit, 2 attention boxes added below;	16ff

Rel.	Rel. Date†	Chapter	Modification	Page
B5	2020-06-16	DESCRIPTION	Note box added	2
		ELECTRICAL CHARACTERISTICS	Items 303, 305, 306, 307: condition reference corrected to 302	7
		REGISTER MAP	Notes added on mandatory programming	14
		SERIAL I^2C INTERFACE	Note boxes added, footnote added on sequential write, text and figures arrangement changed	16, 18
		OPERATING MODES	Description of mode Test 5 updated	23

Rel.	Rel. Date†	Chapter	Modification	Page
C1	2022-06-02	PACKAGING INFORMATION	Footnote 1 updated	4
		ABSOLUTE MAXIMUM RATINGS	Condition added to G001, G002, correction of G010	6
		ELECTRICAL CHARACTERISTICS	Item D06: min limit adapted	7
		CONFIGURATION REGISTERS, MONITORING AND ERROR OUTPUT	Change of headlines to match block diagram Footnote added on voltage dip	14, 39
		SERIAL I^2C INTERFACE	Correction of Figure 5, text deleted in note box #2 and #5	16ff
		INDEX GATING, OUTPUT DRIVERS	Change of headline to match block diagram, contents separated into 2 sections	36, 38

† Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-PI	20-pin TSSOP RoHS compliant	iC-PI TSSOP20
Evaluation Board		iC-PI EVAL MQ1D

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

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Am Kuemmerling 18
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GERMANY

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Fax: +49 (0) 61 35 - 92 92 - 192
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